Very Low Voltage Testing of SOI Integrated Circuits

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Abstract

Very Low Voltage (VLV) testing has been proposed to increase flaw detection in bulk silicon CMOS integrated circuits and this paper explores these and additional advantages in the context of testing Silicon-On-Insulator (SOI) integrated circuits. In the VLV regime, the history effect, which describes how delays through SOI circuits vary based on a circuit's recent switching history, is amplified. This amplification improves the ability at test to monitor fabrication process shifts, which may lead to excessive delay variation under normal operating conditions. VLV test techniques can be used to identify parts that have been fabricated outside the specified process window. In addition, the use of VLV testing is investigated to detect defects that have been described in previous VLV papers, however now addressed in the context of SOI technology.

1. Introduction

As the scaling of traditional bulk CMOS appears to be unable to progress further, Partially-Depleted Silicon-On-Insulator (PD-SOI) technology has begun to garner more industry attention as a vehicle to extend the performance of digital CMOS into the 21st century. By reducing the short channel effects in the deep sub-micron regime, by eliminating parasitic capacitances, and by diminishing the performance reductions caused by the body effect, SOI provides an additional boost in performance for next generation digital applications. SOI has been reported to provide as large as a 20 to 35% increase in performance when compared to bulk technology of the same lithographical dimensions [Chuang98], [Wei98].

However, SOI presents new challenges in terms of design and test of digital circuits. The SOI transistor is identical to the traditional bulk transistor in most aspects with the notable exception that it is fabricated on a buried oxide layer. This oxide layer provides electrical isolation from the substrate and the resulting isolation leads to the floating voltage of the body node. The body voltage is determined by the balance of currents into and out of the body based on the recent switching history of the transistor. What makes this interesting is that the body voltage, which is fixed in bulk silicon CMOS, impacts the threshold voltage of the transistor through the physical phenomenon known as the body effect. The body effect describes how an increase in the body to source voltage decreases the threshold voltage – the gate to source voltage at which inversion sets in resulting in a conducting channel between the source and drain. A change in this threshold voltage has a direct impact on the performance of the transistor, and thus, the floating body in SOI is responsible for a new variation in delay – dependent on the switching history of the transistor - that is not present in traditional bulk CMOS technology.

Very Low Voltage (VLV) testing has been proposed in the past to identify marginal integrated circuits by amplifying the significance of otherwise undetectable flaws. [Hoa93], [Chang96a] and [Chang96b] reported that VLV testing is useful in detecting a variety of defects, which included shifts in the threshold voltage resulting from hot electron degradation or mis-processing. In this paper, the use of VLV testing is examined in terms of amplifying the SOI history effect in order to monitor the extent of the delay variation caused by the floating body. This new test provides a powerful indicator of the extent of the history effect in SOI devices and can be used to identify circuits that were fabricated outside of the specified fabrication process window and would be otherwise undetectable with conventional testing. Having an aggravated history effect, such devices may result in intermittent failures or reliability problems in field applications and this test can provide not only additional flaw coverage at manufacturing test but also be useful as a diagnostic tool for field returns. In addition, VLV testing is also explored with regards to detecting conventional VLV defects in SOI circuits - the effectiveness of which can be strongly affected by the recent switching history of the circuit. In fact, this paper describes how the history effect must be accounted for in the application of the VLV tests. Otherwise, defects can become less manifest at low voltage than under normal operating conditions due to a temporary performance improvement due to the history.

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2. History Dependence of Delay in SOI ICs

SOI technology has existed since the late 1970's – primarily used in military and space applications where SOI's reduced soft error rate was a requirement. More recently, the technology has received more attention in terms of improving performance or reducing dynamic power consumption in consumer electronic applications. In almost every respect, SOI technology is identical to traditional bulk CMOS technology, where the most interesting difference is that the transistor is fabricated on a buried oxide layer as illustrated in Fig. 1. This oxide provides a dramatic reduction in junction capacitance and results in a substantial decrease in the energy - delay product of SOI circuits relative to bulk circuits. By building the transistor on a buried oxide, the body of each transistor is isolated electrically from the bodies of the other transistors in the circuit. Whereas in bulk, the NFET devices share a common P well and PFET devices share an N well, each transistor body in SOI is now floating. As a consequence of the floating body, the body voltage can be raised in the static sense to a diode drop above the source node. This is in stark contrast to bulk technology where the body is statically tied to either V_{dd} or ground through a well tie and this difference leads to several significant departures from traditional bulk transistor behavior.

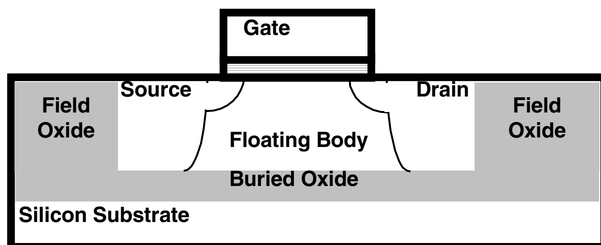

Figure 1 – Cross-Section of the SOI Transistor

One of the consequences of the floating body is that there now exists a relationship between the recent switching history of a digital circuit and the delay through that circuit [Assaderaghi00]. This relationship is based on how the body voltage is modulated as a consequence of the switching of the other terminals of the transistor and, in turn, how the body voltage affects the threshold voltage of that transistor. In the simple example of a chain of inverters as depicted in Fig. 2, if the input to the chain were held low for a long period of time (much longer than the functional cycle time), the body voltages of the NFET transistors in the odd inverters would be increased relative to an analogous bulk inverter chain. This occurs because the reverse bias leakage of the drain-to-body junction charges the body node up until the opposing source-to-body junction is on the verge of forward biasing. At this equilibrium point, the balance of currents from the two junctions is zero and the body voltage hovers around ~0.6V. This positive V_{bs} voltage reduces the threshold voltage. Consequently, these transistors would have temporarily improved performance.

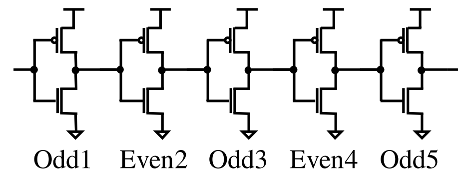

Figure 2 – Example Circuit Data Path

Conversely, the NFET transistors in the even inverters would have both the drain and source terminals at the ground potential (gate node is at a logic one) and this would result in the body voltage being grounded as well. With the body voltage grounded, these NFET transistors would have bulk-like performance (approaching yet still better than bulk) and would be slower than their odd inverter counterparts. A dual relationship exists with the PFET transistors, where the even inverter PFETs would have improved performance while the odd inverter PFET transistors would remain bulk-like.

If subsequently, a rising edge was applied to the input of the inverter chain, the edge would propagate down the chain activating the faster transistors (odd NFETs and even PFETs) and the total propagation delay would be substantially less than if the inverter chain had been fabricated in bulk technology. However, if a falling edge was applied immediately afterwards – completing a full square-wave pulse - the propagation delay would be closer to bulk as the transition would traverse the chain activating the slower transistors. Consequently, the pulse at the output of the chain would be "stretched" relative to the pulse applied to the input. This new phenomenon in SOI is referred to as "pulse stretching" and illustrates how the switching history (input held low for a long period in this case) results in a variation in the delay through the circuit. This variation must be addressed at test to provide the worst-case (slowest) environment during delay testing. A compounding complication of SOI is that for some technologies "pulse shrinking" has been reported [Houston98]. This is due to a reversal in the order of priority of the different currents contributing to the body charge and thus establishing the body voltage [Bernstein00]. In either case, the history effect exists and must be accounted for at test to ensure that a device will work at a given frequency under all specified operating and switching history conditions. Consequently, the use of pre-conditioning is required

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prior to delay testing a critical path to establish a "slow" recent switching history.

In [MacDonald99], a delay test with pre-conditioning was proposed that would ensure the worst-case (slowest) switching history for all transistors in a path to be delay tested. By applying a pre-conditioning pattern for a period long enough to ensure that the body voltages had reached equilibrium, a delay test could be applied which exercises the circuit with all threshold voltages set to the highest or lowest levels based on the recent switching. [MacDonald99] included simulations run on benchmark circuits that illustrated the percentage of variation possible due to the SOI history effect, and depending on the circuit, ranged between 7 and 13%. These percentages were determined by measuring the delay through a path under both best case (fast) and worst-case (slow) switching histories and then calculating the percent change in delay. Both the slow and fast histories were created by pre-conditioning the path and then applying a square wave pulse. The propagation delay precipitated by the first rising edge represented the fast-case rising edge delay, while the following falling edge provided the worst-case falling edge delay – based on the pulse stretching phenomenon. After an additional pre-conditioning period, a second inverted pulse was applied to obtain the worst case rising edge delay and best case falling edge delay in a similar fashion with an inverted pulse. With all four measurements, the delay variation caused by the history effect can be calculated for both the rising and falling propagation delays through the tested path. Although [MacDonald99] only described delay testing at nominal operating conditions (V_{dd} = 2.5V for 0.25u University of Florida SOI spice models), the method of generating an extreme switching history also applies to very low voltages conditions. The only significant difference in the history effect at very low voltages is the reduction of the charge contribution from impact ionization. However, although impact ionization may play a role in a steady state switching scenarios, the delay tests in [MacDonald99] rely on the first and second switch after a static pre-conditioning period and therefore remain unaffected.

3. Proposed VLV Test for SOI Circuits

The sensitivity of a transistor's performance to V_t fluctuations increases as V_{dd} is lowered in either bulk or SOI technology and this is one of the motivations for employing VLV testing [Hoa93] [Chang96a] [Chang96b]. This increased sensitivity can be seen intuitively from the MOSFET drive current equation, where the parenthetic term (V_{gs} –V_t) approaches zero as V_{gs} approaches V_t. The transistor drive current, I_{ds}, is directly proportional to the performance of a transistor and this implies that V_{dd} must be greater than V_t to generate more than subthreshold current (leakage). As V_{dd} is lowered and approaches V_t, the sensitivity of the delay through a circuit to shifts in the threshold voltage increases significantly and this increased sensitivity can provide a mechanism for monitoring the extent of the history effect in SOI circuits.

The history effect manifests itself as local shifts in threshold voltages and has a negligible impact on the operation of a defect-free circuit designed with special attention given for the floating body and fabricated within the specified window of process parameters (i.e. doping, lithographic dimensions, etc.). However, minor variations in several contributing parameters could conspire to increase the influence of the switching history on device operation and result in intermittent failures or degraded performance under specific data-dependent applications. Furthermore, some defects may promote the history effect causing local increases in the extent of the SOI-specific delay variation. These defects could include resistive shorts between any of the transistor's nodes and the body, increasing the influence of the affected node over the body voltage, and consequently aggravating the history effect. Consequently, monitoring the extent of the history effect globally can help identify susceptible parts.

Monitoring the history effect under normal operating conditions (voltage and temperature) is difficult at best for today's high performance devices. By applying delay tests in the VLV regime, the delays and the delay variations become much more significant and easier to measure. Furthermore, by performing delay tests at low voltage, both the fast and slow history delay for the same path can be measured – regardless of the technology being of the stretching or shrinking variety. Having measured path delays under two switching histories allows for the percent variation to be calculated for the path under test. This percent variation is the most directly representative value of the history effect in SOI. Figure 3 illustrates this for the series of inverters. As V_{dd}

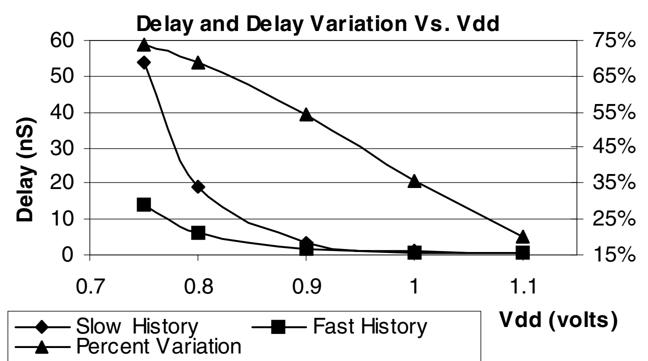

Figure 3 – Delay Vs. V_{dd} and Two Switching Histories

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bis decreased both the absolute magnitude of the delay, the magnitude of the difference of delays for different switching histories and the percent variation all increase, and thereby allow for devices with increased history influence to be more readily detected.

The use of VLV testing can be used to ensure that the extent of the history effect is within specification. The sensitivity of the history-dependent fluctuations in the V_t can be amplified without the need for higher performance test equipment, and thus devices with a history dependence that is out of specification can be identified more easily. As an example, Fig. 4 describes the delay variation for the series of inverters across a range of gate oxide thickness (T_{ox}), a tightly controlled process parameter, which influences the history effect. For these simulations models, T_{ox} is set to a nominal 56 angstroms and Fig. 4 illustrates how a change as small as a single angstrom can influence the history effect significantly at very low voltages. The history dependence increases the gamma coefficient of the body effect is increased with increased T_{ox}. Although the corresponding increase in the history effect at nominal voltages is difficult to measure based on the small magnitude of the delay variation, it may be enough to cause intermittent failures as untested, critical paths are extended past the functional cycle due to the history dependence.

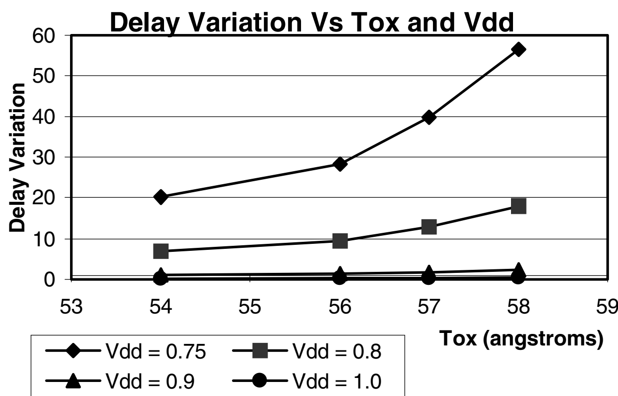

Figure 4 – Delay Variation Vs. T_{ox} and V_{dd}.

4. Effectiveness of VLV Test for SOI Circuits

In addition to monitoring shifts in the fabrication process that affect the extent of the history dependence, VLV testing of SOI circuits can also be exploited for identifying traditional VLV defects. [Chang96b] described several specific defects that were more easily identified with VLV testing and these defects include transmission gate opens, gate oxide shorts, metal shorts and hot carrier degradation. In the case of each defect in which delay testing is necessary, the switching history must be considered for VLV testing, otherwise a fast history may mask a defect by temporarily improving the performance of a path. In fact, the defect may become more difficult to detect in the VLV regime - where the history effect is amplified - than it is in the normal operating voltage range defeating the original purpose of VLV testing. Ensuring that a path is tested under the worst-case (slow – high V_t) switching history becomes even more important in the context of VLV testing and the delay testing techniques described in [MacDonald99] provide a mechanism for creating the worst-case switching history. These techniques still apply in the VLV regime and should be employed for VLV delay tests of static circuits. Transmission gate defects, on the other hand, require closer scrutiny with regards to the switching history to ensure the effectiveness of VLV testing.

[Chang96b] describes a transmission gate open defect - in which the PFET transistor (*I2* in Fig. 5) in a complimentary transmission gate becomes "stuck off" – causing logic high levels to be reduced by the magnitude of an NFET V_t at an intermediate output (net *out_n* in Fig. 5). This degradation is manifested as increased delay with the delay becoming even more significant at very low voltages based on the fact that the V_t degradation does not scale with V_{dd}. The defect becomes detectable by a simple DC boolean test if the degraded logic high level never crosses the switching threshold of the output inverter. This switching threshold scales with V_{dd}, however the degradation resulting from the defect is always a V_t drop regardless of the value of V_{dd}. Consequently, the lower the V_{dd}, the more effective the VLV test becomes.

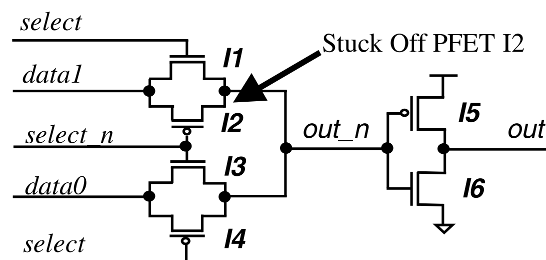

Figure 5 – Faulty Transmission Gate with Missing PFET

In SOI technology, the degradation described above has a strong history dependence because the V_t is strongly affected by the body to source voltage. In fact, pass transistor configurations are considered "high leverage" circuits in SOI due to the decrease in the body effect (in the traditional sense) relative to bulk as well as the decrease in junction capacitance on the source node, which is now used as an input. However, the "high

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leverage" nature of pass transistors in SOI makes them more prone to the history dependence of the threshold voltage [Puri00]. Figure 6 shows the waveforms of the circuit in Fig. 5 in which the alternative input (*data0*) makes a transition just prior to the *select* signal asserting. As a result of the drain and source of *I1* being held high for a long time (initial conditions), the body voltage of the transistor begins at V_{dd}. When *select* asserts, the body is capacitively coupled above V_{dd}, reducing the V_t and improving the signal degradation.

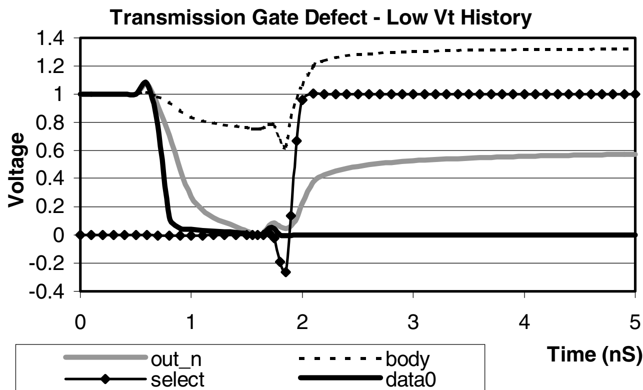

Figure 6 - Faulty Transmission Gate - Low V_t history

Conversely, in Fig. 7, the alternative data input (*data0*) is held low through out the simulation while the input (*data1*) starts low and transitions high. As a consequence of the drain and source being held to the ground potential for the recent history, the body voltage of *I1* is also at ground. When the *select* signal asserts, the body is capacitively coupled up, but based on the starting point, the body voltage never exceeds the value of V_{dd} and consequently the V_t is much higher than in the previous history example. This, in turn, leads to more signal degradation – as much as 100 mV, which for this defective circuit resulted in an increase of 200nS in delay.

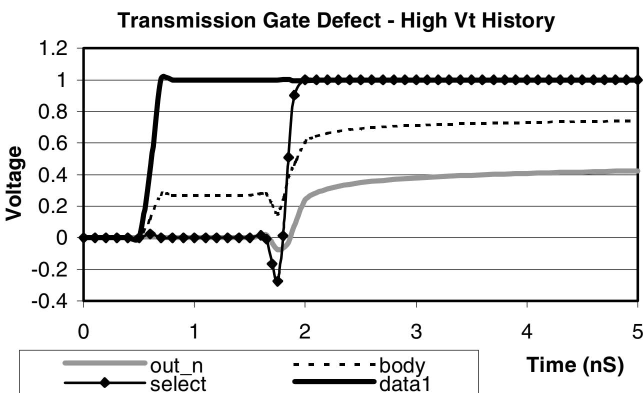

Figure 7 – Faulty Transmission Gate – High V_t history

5. Temperature / Voltage Selection

In [Chang96a], a methodology was described for 0.8 and 0.6 um bulk technology for the selection of an effective V_{dd} for very low voltage testing. The range of V_{dd} was established by considering the tradeoffs between flaw coverage (resistance of defect detected), test time, and noise margins. For these technologies, the acceptable range of supply voltage was based on a ratio with the threshold voltage. The case of SOI technology, however, is complicated by the fact that the threshold voltage is dynamic and depending on the switching history, each transistor has a unique value. Threshold voltages, in general, can range from 0 volts (very high body to source voltage) to near the nominal value, V_{t0} (body to source voltage equals zero). For delay testing in the VLV regime, the use of the original VLV guidelines using a ratio of V_{dd} to the nominal threshold voltage is appropriate if the switching history is accounted for by using the techniques described in [MacDonald99] for delay testing. Otherwise the effectiveness of VLV delay testing may be compromised for cases where the threshold voltages are reduced, and in fact, defects that are deemed detectable by delay testing may become less manifest in the VLV regime than under normal operating conditions.

In [Chang96a], two sets of boolean tests were simulated: 1) a NAND gate with a gate oxide short and 2) a metal short between two outputs of inverters in separate inverter chains. Acceptable flaw coverage (resistance detected) in the case of both gate oxide shorts and metal resistive shorts was targeted to be at least 5K ohms, which represents the vast majority of both of these defect types. This provided an effectiveness metric that determined the upper end of an acceptable range of supply voltage values for very low voltage testing. Similar simulations were performed with SOI models using the same boolean tests and the results generally agree with the conclusions drawn in the previous paper. In SOI technology, the supply voltage should be no higher than 2.3 times the threshold voltage to provide comparable flaw coverage to that reported in [Chang96a] as illustrated in Fig. 8. The reduction in the upper limit from 2.5 to 2.3 can be accounted for by the general reduction in V_t for the SOI circuits. In boolean tests, the static input values tend to cause the active transistors to approach but never quite reach the nominal threshold, V_{t0}. Thus the ratio of V_{dd} to V_t is more conservative for this technology.

To determine the lower limit of the supply voltage, test time was considered. From Fig. 3, it is clear that approximately two times the nominal threshold voltage (V_{t0} = 0.42 V in SOI simulations) is where delays begin to increase significantly for SOI. Any increase in delay for a good device must be accounted for and reconciled in

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the test frequency of the very low voltage testing and undue increases will increase the overall test time of the device. This, of course, results in increased cost. Therefore, SOI is similar to the technologies described in [Chang96a] and the lower limit of the supply voltage should be maintained above two times the nominal threshold voltage based on test time considerations.

[Puri01] discusses the effects of temperature on the history effect in SOI and describes how as the temperature is increased, the history effect is diminished as the body voltages tend to be forced to the slow / high V_t corner due to increased leakage and electron-hole generation in the body. Given that traditional VLV defects are generally aggravated at higher temperatures, than it follows that for SOI, traditional VLV tests should be performed at the highest specified temperature allowed for the technology. This may allow for the elimination of pre-conditioning paths if the temperature can be raised sufficiently to minimize the history effect to negligible levels. Conversely, for the test proposed in Section 3, the temperature should be reduced to the lowest possible level to increase the history effect and improve the probability of detecting devices that are out of specification with regards to the influence of the floating body on the performance of the circuit.

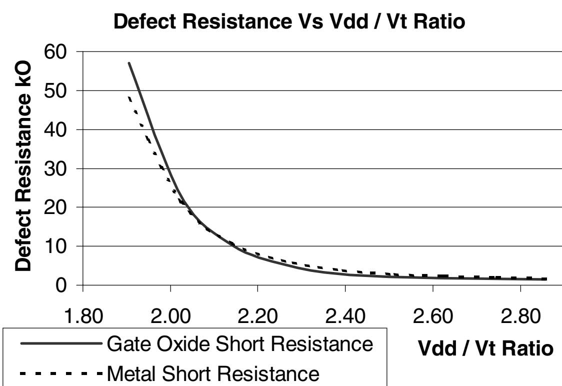

Figure 8 – Defect Resistance Detected Vs. V_{dd} / V_t Ratio

6. Conclusions

Very low voltage testing has been proposed in the past for bulk CMOS technology as an inexpensive test technique for either production testing or diagnostics. Using existing test equipment, VLV testing can provide coverage for defects that pass testing at the nominal operating range but otherwise could cause early life or intermittent failures. This paper has proposed an extension to the use of very low voltage testing for SOI CMOS technology to monitor the extent of the history effect. By providing an indication if a device has been fabricated outside a range causing an unacceptable delay variation, intermittent failures due to the history effect can be avoided.

Additionally, this paper has examined the effectiveness of VLV testing in SOI technology for detecting the traditional (bulk technology) defects described in previous literature and has shown that the switching history must be accounted for to ensure that VLV testing is fully exploited. The guidelines for applying very low voltage testing remain roughly the same for SOI circuits with two exceptions. First, the supply voltage range is more restrictive and should be set between 2.0 and ~2.3 times the value of the nominal (V_{bs} = 0) threshold voltage. This is because the floating body in SOI results in a general reduction in the V_t from the nominal value under most conditions and this reduces the maximum ratio of supply voltage to threshold voltage. Second, the history effect must be accounted for in delay testing, because a best case switching history may mask the effects of a delay flaws at very low voltage and these flaws may become less manifest in the VLV regime, thus defeating the original motivation for VLV testing.

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