

**Writing embedded systems code in C using Metrowerks**

**Installation**  
**Projects**  
**Mixed C/assembly**  
**PLL**  
**Debugger**  
**Importing TExaS code from previous labs**  
**Exporting object code to simulate in TExaS**

**Installation**

**9S12/Metrowerks link**  
<http://users.ece.utexas.edu/~valvano/S12C32.htm>  
**How to download Metrowerks**

**StarterFiles**

**xxxx\_DP512.zip** is a DP512 Metrowerks project  
**xxxx\_DP512asm.zip** is a DP512 TExaS example

**Projects, look at an example starter file, OC\_DP512.zip****See Folders**

**Sources** programs  
**bin** object code, TExaS files  
**xxx.mcp** project, can double click this  
 Source code files (you create these) (text)  
**xxx.asm** assembly source  
**xxx.c** C source code file  
**xxx.h** C header file  
 Object code files (created when you compile) (text)  
**xxx.lst** multiple assembly listing files  
**HCS12\_Serial\_Monitor.map** symbol table  
**HCS12\_Serial\_Monitor.sx** object code

**Create a new project****Add a new file called pll.asm**

```

SYNR      equ $0034 ; CRG Synthesizer Register
REFDV     equ $0035 ; CRG Reference Divider Register
CRGFLG    equ $0037 ; CRG Flags Register
CLKSEL    equ $0039 ; CRG Clock Select Register
PLLCTL    equ $003A ; CRG PLL Control Register

          absentry PLL_Init
;***** PLL_Init *****
; Active PLL so the 9S12 runs at 24 MHz
; Inputs: none
; Outputs: none
; Errors: will hang if PLL does not stabilize
PLL_Init
  movb #$02,SYNR      ; 9S12DP512 OSCCLK is 16 MHz
  movb #1,REFDV
  movb #0,CLKSEL      ; PLLCLK = 2 * OSCCLK * (SYNR + 1) / (REFDV + 1)
  movb #$D1,PLLCTL   ; Clock monitor, PLL On, high bandwidth filter
  brclr CRGFLG,$08,* ; wait for PLLCLK to stabilize.
  bset CLKSEL,$80    ; Switch to PLL clock
  rts

```

**Add this to main**

```
void PLL_Init(void);
```