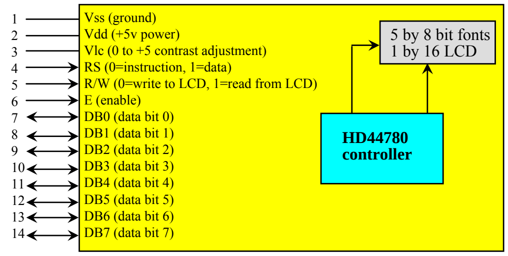


Lecture 7 objectives

- HD44780 review
- digital logic families
- input/output voltage/current
- PN2222 NPN transistor interface of a speaker

8.3.4. LCD interface with the HD44780 controller

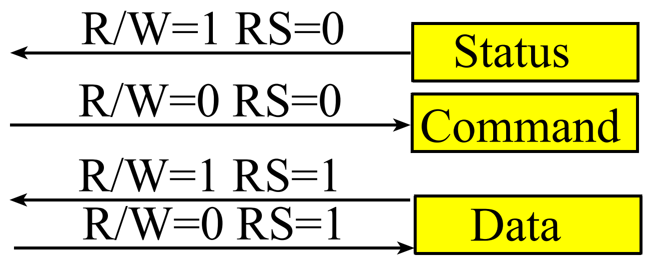


Figure 8.55. Interface of a HD44780 LCD controller.

There are four types of HD44780 cycles

RS	R/W	Cycle
0	0	Write to Instruction Register
0	1	Read Busy Flag (bit 7)
1	0	Write data from µP to the HD44780
1	1	Read data from HD44780 to the µP

Table 8.8. Two control signals specify the type of access to the HD44780.

Show `LCD.pdf` `hd44780.pdf` LCD project

Lab 3. Alarm clock	**shows the time**
Lab 4. Stepper motor	**optional debugging monitor**
Lab 5. SPI DAC tone	**optional debugging monitor**
Lab 6. Thermometer	**displays temperature**
Lab 9. Capacitance	**displays capacitance**
Lab 10. ZigBee	**displays message on receiver**
Labs 8,11. Project	**display for system**

How to read busy flag,

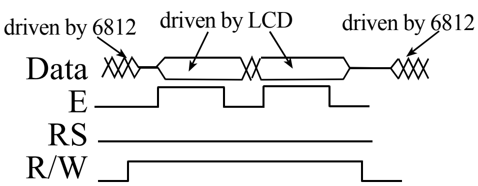
Decide on a default settings. E.g.,

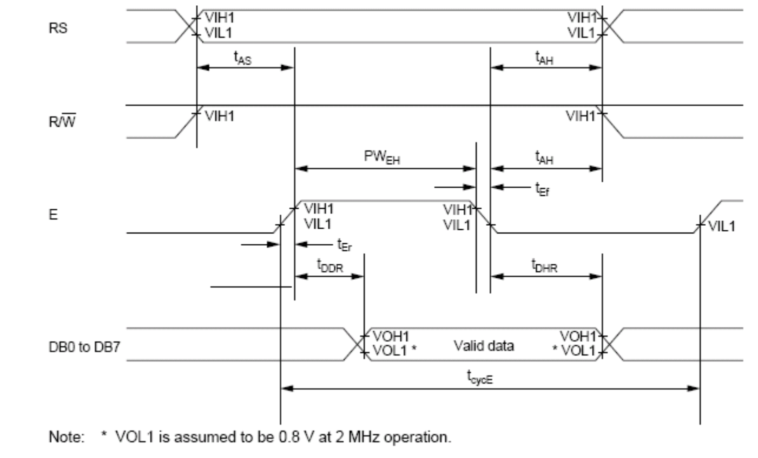
4-bit data direction = 0x0F (output),
E=0 (off)
RS = 0 (command)
R/W = 0 (write)

Execute the initialization routine using blind-cycle

4-bit protocol read Busy

1) data direction input on the 4 data bits (3 control bits remain output)
2) R/W=1, RS=0
3) E=1
4) Wait a little time (2 nops) [it does not work without delay]
5) Read 4-bit MS nibble data (bit 3 is busy)
6) E=0
7) E=1
8) Wait a little time (2 nops)
9) Read 4-bit LS nibble data (nothing interesting)
10) E=0
11) R/W=0 (default settings)
12) direction on 4 data bits back to output (default settings)



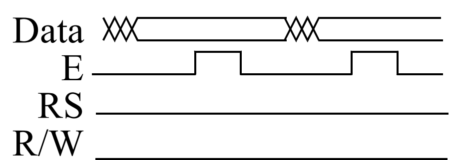


LCDHD44780.pdf

Figure 28 Read Operation

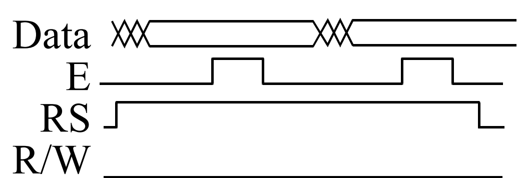
4-bit protocol write command (`outCsr` in LCD starter file)

- **0) wait for BUSY=0 (idle), fail if not idle within 2ms**
- **1) set 4-bit MS nibble data port with command info**
- **2) E=1**
- **3) Wait a little time (2 nops) [it does work without delay]**
- **4) E=0**
- **5) set 4-bit LS nibble data port with command info**
- **6) E=1**
- **7) Wait a little time (2 nops) [it does work without delay]**
- **8) E=0 (default settings)**



4-bit protocol write ASCII data (`LCD_OutChar` in LCD starter file)

- **0) wait for BUSY=0 (idle), fail if not idle within 100us**
- **1) RS=1**
- **2) set 4-bit MS nibble data port with ASCII character**
- **3) E=1**
- **4) Wait a little time (2 nops) [it does work without delay]**
- **5) E=0**
- **6) set 4-bit MS nibble data port with ASCII character**
- **7) E=1**
- **8) Wait a little time (2 nops) [it does work without delay]**
- **9) E=0**
- **10) RS=0 (default settings)**



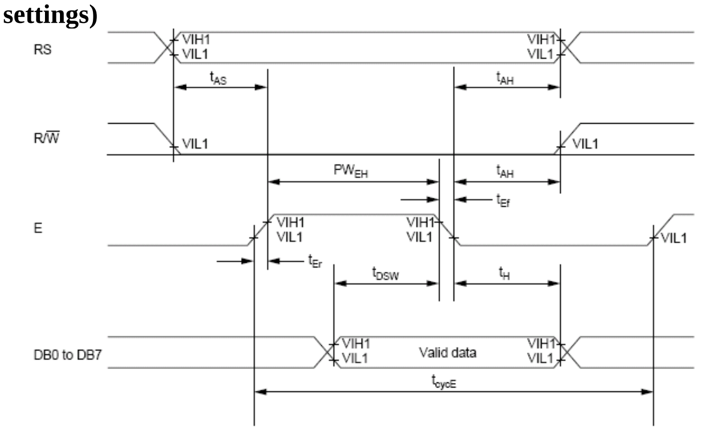


Figure 27 Write Operation

LCDHD44780.pdf

1.6. Digital Logic and Open Collector

Normal digital logic has two states. There are four currents of interest when analyzing if the inputs of the next stage are loading the output. I_{IH} and I_{IL} are the currents required of an input when high and low respectively. Similarly, I_{OH} and I_{OL} are the maximum currents available at the output when high and low.

In order for the output to properly drive all the inputs of the next stage, the maximum available output current must be larger than the sum of all the required input currents for both the high and low conditions.

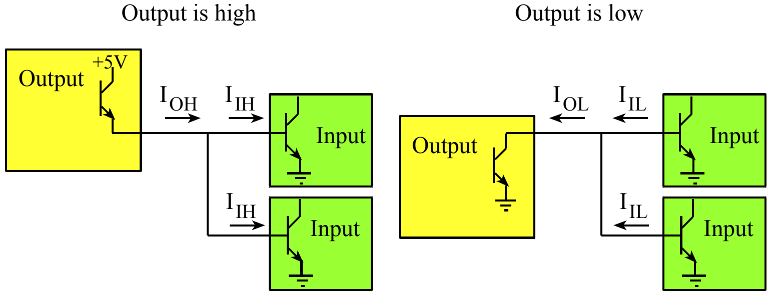


Figure 1.55. Sometimes one output must driver multiple inputs.

fan out as the maximum number of inputs, one output can drive.

fan out = minimum((I_{OH}/I_{IH}) , (I_{OL}/I_{IL}))

For circuits that mix devices from one family with another, we must look individually at the input and output currents, voltages and capacitive loads. The following table shows typical current values for the various digital logic families.

family	example	I_{OH}	I_{OL}	I_{IH}	I_{IL}	fan out
standard TTL	7404	0.4 mA	16 mA	40 µA	1.6 mA	10
Schottky TTL	74S04	1 mA	20 mA	50 µA	2 mA	10
Low Power Schottky	74LS04	0.4 mA	4 mA	20 µA	0.4 mA	10
High speed CMOS	74HC04	4 mA	4 mA	1 µA	1 µA	
Freescale	68HC812A4	0.8 mA	1.6 mA	1 µA	1 µA	
Freescale	**9S12DP512**	**0.8 mA**	**1.6 mA**	**1 µA**	**1 µA**	

Table 1.3. The input and output currents of various digital logic families.

The following figure compares the input and output voltages for many of the digital logic families. The four parameters that affect our choice of logic families are

- power supply current
- speed
- output drive, I_{OL}, I_{OH}
- noise immunity

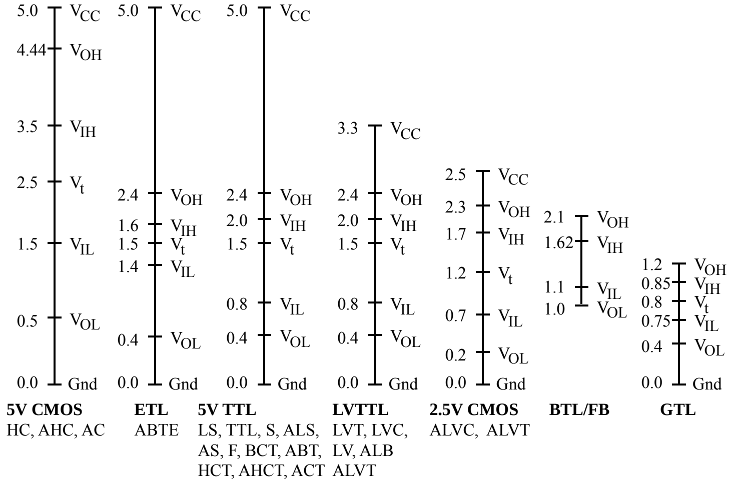


Figure 1.13. Voltage thresholds for various digital logic families.

The 74LS04 is a low-power Schottky NOT gate. The output is *high* when there is active transistor, Q4, driving the output to +5V. The output is *low* when there is an active transistor, Q5, driving the output to 0.

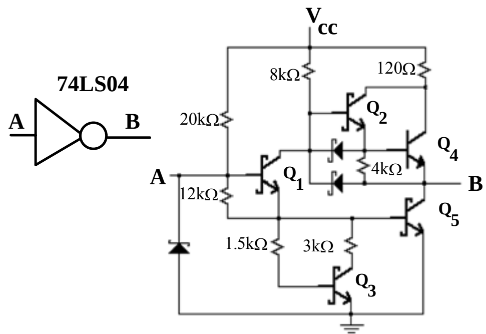


Figure 1.15. Transistor implementation of a low-power Schottky NOT gate.

The 74HC04 is a high-speed CMOS NOT gate.

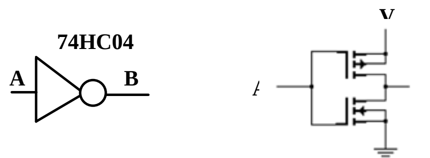


Figure 1.16. Transistor implementation of a high speed CMOS NOT gate.

Open collector or open drain logic outputs also have two states.
The output is *open* when there is no active transistor driving the output.
The output is low when there is an active transistor, Q3, driving the output to 0.

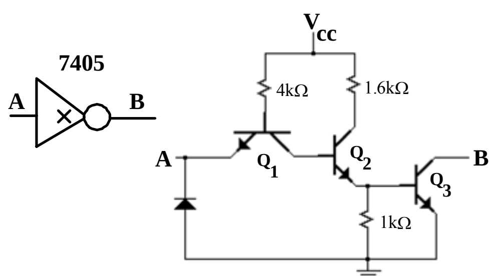


Figure 1.17. Transistor implementation of a regular TTL open collector NOT gate.

The 74HC05 is a high-speed CMOS open collector NOT gate.

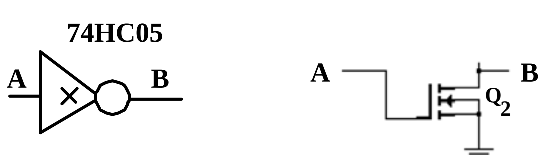


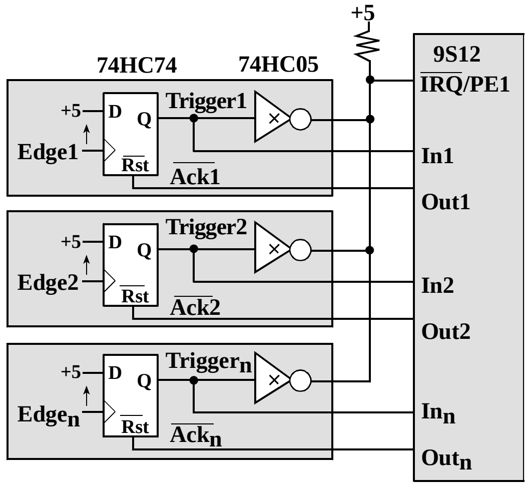
Figure 1.18. Transistor implementation of a high speed CMOS open collector NOT gate

Multiple uses of open collector

Current switch (LED, relay, motor, stepper motor)
Logical function (IRQ interrupt request, PE1)
Multidrop network

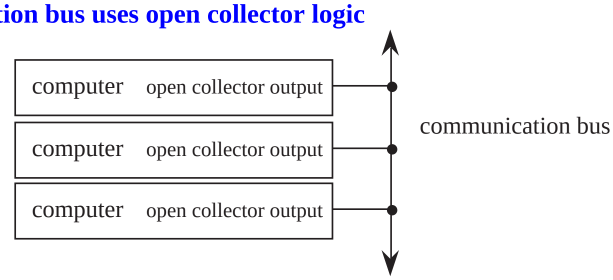
This IRQ interface uses open collect logic for the interrupt request

Shared IRQ vector (polled interrupt)
Separate ability to read trigger flag (ISR must poll)
Separate ability to clear trigger flag (acknowledge)



Many microcomputers can implement open collector logic.

This bidirectional communication bus uses open collector logic



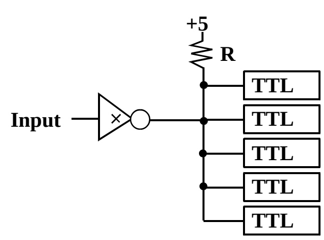
Open collector implementation of a half-duplex communication network.

pullup resistor

the smaller the resistor, the larger the I_{OH} when the output is high.
a larger resistor does not waste as much I_{OL} current when the output is low.

1) determine the required output high voltage, V_{out},
2) determine the output high current, I_{out}
3) the resistor must be less than:

$R \le (+5 - V_{out})/I_{out}$



Calculate the resistor value to drive five regular TTL loads.

V_{out} must be above V_{IH} (2 V) in order for the TTL inputs to sense a high
Safety factor and set V_{out} at 3V.
I_{out} must be more than five I_{IH}.
I_{IH} is 40 µA, so I_{out} should be larger than 5•40 µA or 0.2mA.
$R \le (5\text{-}3V)/0.2mA = 10\ k\Omega$.

Calculate the resistor value to interface these switches

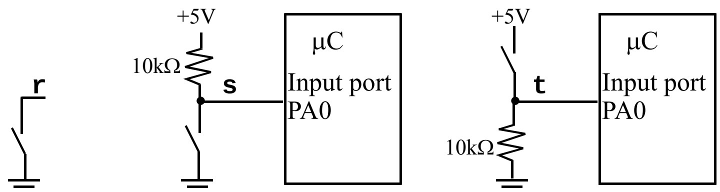


Figure 1.20. Switch interface.

V_{out} must be above V_{IH} (3.5 V) in order for the TTL inputs to sense a high
Safety factor and set V_{out} at 4.9V.
I_{out} must be more than I_{IH}.
I_{IH} is 1 μA, so I_{out} should be larger than 1 μA
$R \leq (5-4.9V)/ 1\ \mu A = 100\ k\Omega$.

A second thought about pull-up resistors, a B3F switch has

On resistance of less than 0.1 Ω
Off resistance of more than 100 MΩ
10 kΩ is close to the geometric mean of 0.1Ω and 100MΩ (3.2 kΩ)

The model for the bipolar NPN transistor is

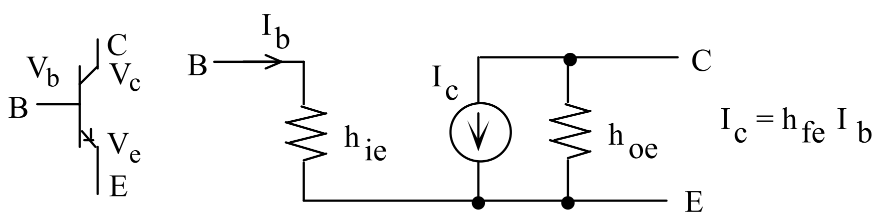


Figure 8.59. NPN transistor model.

There are five basic design rules when using individual bipolar NPN transistors in saturated mode:

1) Normally $V_c > V_e$
2) Current can only flow in the following directions
   from base to emitter (input current)
   from collector to emitter (output current)
   from base to collector
      (doesn't usually happen, but could if $V_b > V_c$)
3) Each transistor has maximum values should not be exceeded
   I_b I_c V_{ce} and $I_c \bullet V_{ce}$
4) The transistor acts like a current amplifier
   $I_c = h_{fe} \bullet I_b$
5) The transistor will activate if $V_b > V_e + V_{be(SAT)}$
   where $V_{be(SAT)}$ is typically above 0.6V

wide range of bipolar transistors that we can use.

Type	NPN	PNP	package	V_{beSAT}	V_{ceSAT}	h_{fe} min/max	I_c
general purpose	2N3904	2N3906	TO-92	0.85 V	0.2 V	100	10mA
general purpose	PN2222	PN2907	TO-92	1.2 V	0.3 V	100	150mA
power transistor	TIP29A	TIP30A	TO-220	1.3 V	0.7 V	15/75	1A
power transistor	TIP31A	TIP32A	TO-220	1.8 V	1.2 V	25/50	3A
power transistor	TIP41A	TIP42A	TO-220	2.0 V	1.5 V	15/75	3A
power darlington	TIP120	TIP125	TO-220	2.5 V	2.0 V	1000 min	3A

Table 8.9. Parameters of typical transistors.

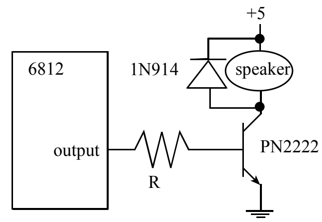



Figure 3.3. 2.25" 32 OHM SPEAKER. 0.38" thick (Lab 3).

Assume 9S12 output at 5V (*see Table 1.13* at least 4.44V)
At saturation (maximum loudness) (*see Table 8.9.*)

V_{BE} = 1.2V

V_{CE} = 0.3V

Ohms Law across speaker

I_{CE} = (5-0.3V)/32Ω = 150mA (right at maximum!)

P = I_{CE}^2*32Ω = 0.72 watts (too loud)

Transistor gain is 100

I_B =I_{CE} /100 = 1.5mA

Ohms Law across input resistor

R = (5-1.2V)/0.0015A = 2500Ω

What if R = 10kΩ?

I_B =(5-1.2V)/10000Ω = 0.4mA

h_{ie} = 2kΩ (not a fixed value)

I_B =V_{OH}/(R +h_{ie}) =5V/(10000Ω +2000Ω)= 0.4mA

Transistor gain is 100

I_{CE} =I_B *100 = 40mA

P = I_{CE}^2*32Ω = 0.05 watts (nice)

PT2 output to speaker, Show Alarm clock signals from Lab 3
Show waveforms on scope

Bottom Line

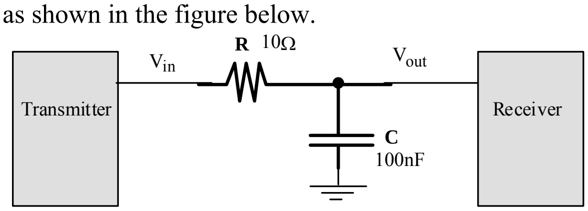
R - Resistive loads require current amplification

L - Inductive loads produce back EMF (snubber diode)

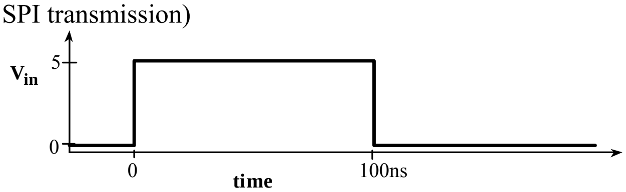
C - Capacitive loads will slow down dV/dt (τ = R*C)

Make it go faster by decreasing R, increasing I

(8) Question 7. The SPI ports of two 9S12s are connected with a VERY long cable. We will model this cable as a single resistor in series with a capacitor, as shown in the figure below.



For this question, assume an ideal transmitter (output impedance of 0) and an ideal receiver (input impedance of infinity). Let **R**=10Ω, and **C**=100nF. Note that R*C is 1µs. Consider a 5V 100ns pulse on the output of the transmitter (labeled as $\mathbf{V_{in}}$) (as might occur with a 5 Mbps SPI transmission)



Derive an equation for $\mathbf{V_{out}}$ as a function of time for the first 100 ns. Show your work and plug in values for R*C is 1µs.