

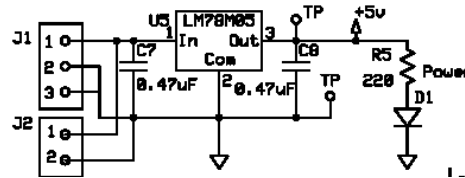
Lecture 20 objectives

- 3.3V voltage regulator
- Interfacing 3.3V and 5.0V logic
- Virtual SCI port using Port T
- Fifo Queue Analysis

Regulator

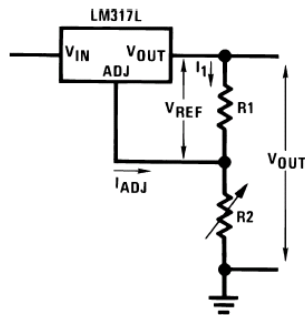
- Output Voltage
- Output Current
- Package
- Cost
- Drop out voltage
- Fixed voltage or adjustable

LM78M05 (TO220 package), $I_{out} = 0.5A$

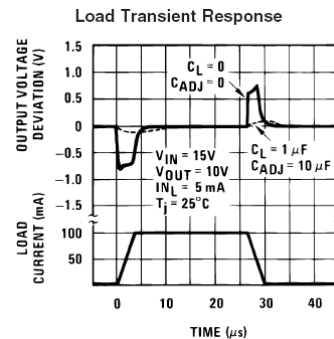
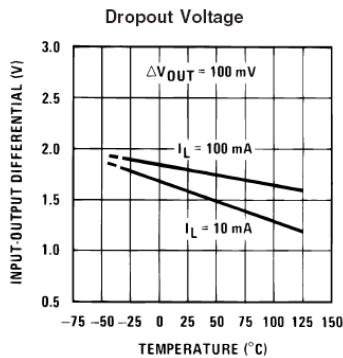
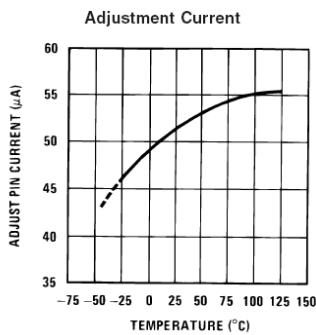
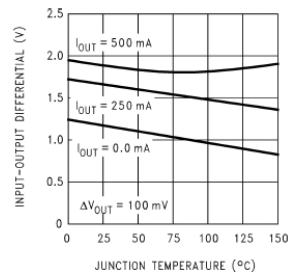


LM317LZ (TO92 package), $V_{REF} = 1.25V$

$$V_{OUT} = V_{REF} \left(1 + \frac{R2}{R1} \right) + I_{ADJ}(R2)$$



Dropout Voltage



ST L4931CZ33

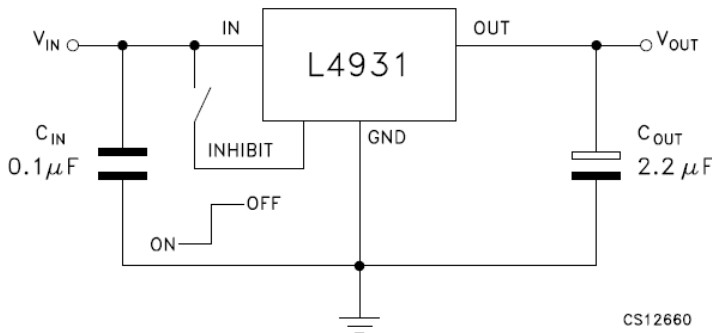
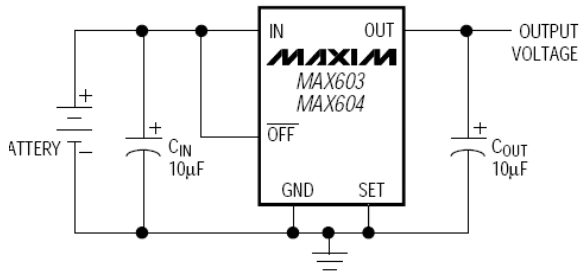


Table 8. Electrical characteristics of L4931Cxx33 (refer to the test circuits, $T_A = 25^\circ\text{C}$, $C_I = 0.1 \mu\text{F}$, $C_O = 2.2 \mu\text{F}$ unless otherwise specified).

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_O	Output voltage	$I_O = 5 \text{ mA}$, $V_I = 5.3 \text{ V}$	3.234	3.3	3.366	V
V_I	Operating input voltage	$I_O = 5 \text{ mA}$, $V_I = 5.3 \text{ V}$, $T_A = -25$ to 85°C	3.169		3.432	V
I_{out}	Output current limit			900		mA
ΔV_O	Line regulation	$V_I = 4.1$ to 20 V , $I_O = 0.5 \text{ mA}$		3	19	mV
ΔV_O	Load regulation (1)	$V_I = 4.3 \text{ V}$, $I_O = 0.5$ to 250 mA		3	18	mV
I_q	Quiescent current ON MODE	$V_I = 4.3$ to 20 V , $I_O = 0 \text{ mA}$		0.6	1	mA
	OFF MODE	$V_I = 4.3$ to 20 V , $I_O = 250 \text{ mA}$		4	6	mA
	OFF MODE	$V_I = 6 \text{ V}$		50	100	μA
SVR	Supply voltage rejection	$I_O = 5 \text{ mA}$	$f = 120 \text{ Hz}$	73		dB
		$V_I = 5.3 \pm 1 \text{ V}$	$f = 1 \text{ kHz}$	70		
			$f = 10 \text{ kHz}$	55		
eN	Output noise voltage	$B = 10 \text{ Hz}$ to 100 kHz		50		μV
V_S	Dropout voltage (1)	$I_O = 250 \text{ mA}$		0.4	0.6	V
		$T_A = -40$ to 125°C			0.8	
V_{IL}	Control input logic low	$T_A = -40$ to 125°C			0.8	V
V_{IH}	Control input Logic High	$T_A = -40$ to 125°C	2			V
I_i	Control input current	$V_I = 6 \text{ V}$, $V_O = 6 \text{ V}$		10		μA
C_O	Output bypass capacitance	$\text{ESR} = 0.1$ to $10 \mu\Omega$, $I_O = 0$ to 250 mA	2	10		μF

1. For 50-8 package the maximum limit of load regulation and dropout is increased by 20 mV.

Maxim MAX603



ELECTRICAL CHARACTERISTICS

($V_{IN} = 6 \text{ V}$ (MAX603) or 4.3 V (MAX604), $C_{IN} = C_{OUT} = 10 \mu\text{F}$, OFF = V_{IN} , SET = GND, $T_J = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_J = +25^\circ\text{C}$.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS				UNITS	
			MIN	TYP	MAX		
Input Voltage	V_{IN}	SET = OUT, $R_L = 1 \text{ k}\Omega$	MAX60_C	2.7	11.5	V	
			MAX60_E	2.9	11.5		
			MAX60_M	3.0	11.5		
Output Voltage (Note 2)	V_{OUT}	$I_{OUT} = 20 \mu\text{A}$ to 500 mA , $6.0 \text{ V} < V_{IN} < 11.5 \text{ V}$	MAX603	4.75	5.00	5.25	V
		$I_{OUT} = 20 \mu\text{A}$ to 300 mA , $4.3 \text{ V} < V_{IN} < 11.5 \text{ V}$	MAX604	3.15	3.30	3.45	
Load Regulation	ΔV_{LDR}	$I_{OUT} = 1 \text{ mA}$ to 500 mA	MAX603C/E	60	100	mV	
			MAX603M		150		
			MAX604	30	100		
Line Regulation	ΔV_{LNR}	$(V_{OUT} + 0.5 \text{ V}) \leq V_{IN} \leq 11.5 \text{ V}$, $I_{OUT} = 25 \text{ mA}$		7	40	mV	
					130		220
Dropout Voltage (Note 3)	ΔV_{DO}	$I_{OUT} = 200 \text{ mA}$	MAX603	$I_{OUT} = 500 \text{ mA}$	320	550	mV
				$I_{OUT} = 200 \text{ mA}$	240	410	
			MAX604	$I_{OUT} = 200 \text{ mA}$	460	820	
				$I_{OUT} = 400 \text{ mA}$			

Logic Conversion

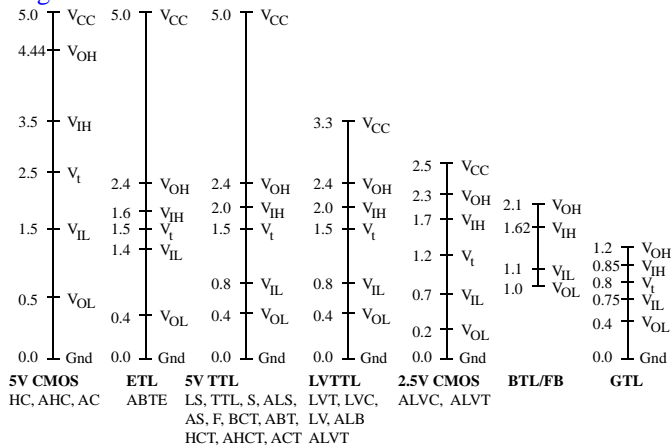


Figure 1.13. Voltage thresholds for various digital logic families.

XBee parameters

9S12DP512 parameters

$I_{OL} = 10 \text{ mA}$, $I_{OH} = 10 \text{ mA}$, $I_{IL} = 1 \mu\text{A}$, $I_{IH} = 1 \mu\text{A}$,
 $V_{OL} = 0.8 \text{ V}$, $V_{OH} = 4.2 \text{ V}$, $V_{IL} = 1.75 \text{ V}$, $V_{IH} = 3.25 \text{ V}$

How to make 9S12 Open collector

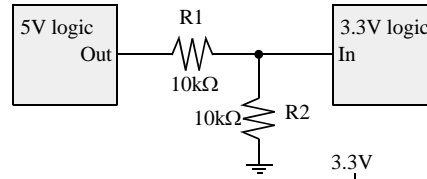
Set Port data bit to zero, once
 When want a low, make DDR bit high
 When want a hiZ, make DDR bit low

Table 1-03. DC Characteristics ($V_{CC} = 2.8 - 3.4 \text{ VDC}$)

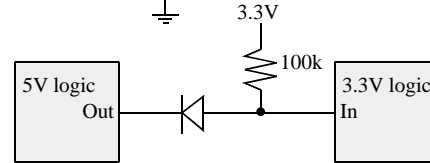
Symbol	Characteristic	Condition	Min	Typical	Max	Unit
V_{IL}	Input Low Voltage	All Digital Inputs	-	-	$0.35 \cdot V_{CC}$	V
V_{IH}	Input High Voltage	All Digital Inputs	$0.7 \cdot V_{CC}$	-	-	V
V_{OL}	Output Low Voltage	$I_{OL} = 2 \text{ mA}$, $V_{CC} \geq 2.7 \text{ V}$	-	-	0.5	V
V_{OH}	Output High Voltage	$I_{OH} = -2 \text{ mA}$, $V_{CC} \geq 2.7 \text{ V}$	$V_{CC} - 0.5$	-	-	V
I_{IH}	Input Leakage Current	$V_{IH} = V_{CC}$ or GND, all inputs, per pin	-	0.025	1	μA
I_{OZ}	High Impedance Leakage Current	$V_{IH} = V_{CC}$ or GND, all I/O High-Z, per pin	-	0.025	1	μA
TX	Transmit Current	$V_{CC} = 3.3 \text{ V}$	-	45 (XBee)	215 (PRO)	mA
RX	Receive Current	$V_{CC} = 3.3 \text{ V}$	-	50 (XBee)	55 (PRO)	mA
PWR-DWN	Power-down Current	SM parameter = 1	-	< 10	-	μA

5 V output, 3.3 V input

- 1) Some chips can support 5V high inputs
- 2) Resistor divider (voltage reducer circuit)



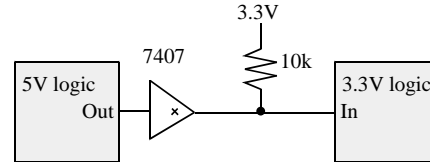
- 3) Schottky diode (fast and low voltage drop)



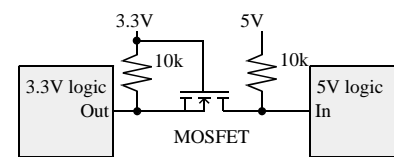
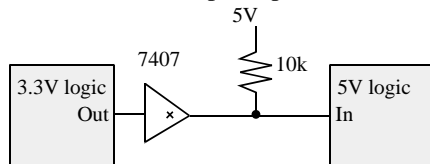
- 4) Open collector with 3.3V resistor pull-up

3.3 V output, 5 V input

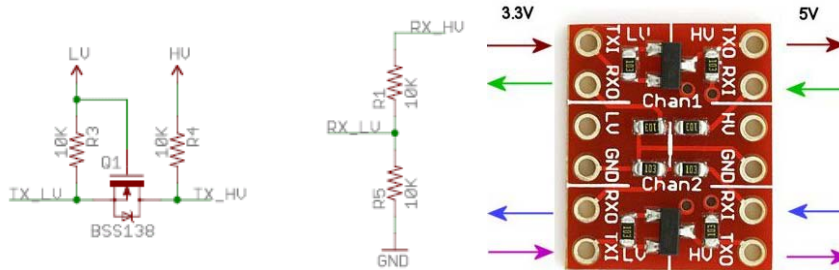
- 1) Some chips can support 3.3V high inputs
- 2) MOSFET (connects the lows, floats the highs)



- 3) Open collector with 5V resistor pull-up



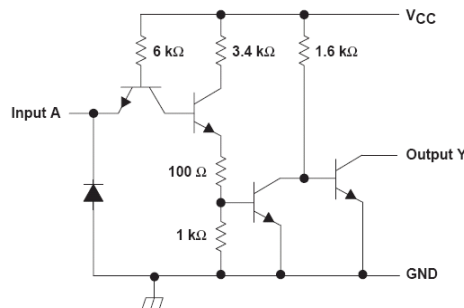
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<http://focus.ti.com/lit/ds/symlink/sn74lvc4245a.pdf>
http://www.maxim-ic.com/appnotes.cfm/an_pk/3007
<http://www.rocketnumbernine.com/2009/04/10/5v-33v-bidirectional-level-converter/>



Sparkfun BOB-08745

<http://www.fairchildsemi.com/ds/BS/BSS138.pdf>

TTL Open collector logic, e.g., 7407



7407 parameters

$I_{OL} = 40\text{mA}$, $I_{OH} = \text{none}$, $I_{IL} = 1.6\text{mA}$, $I_{IH} = 40\mu\text{A}$,
 $V_{OL} = 0.7\text{V}$, $V_{OH} = \text{none}$, $V_{IL} = 0.8\text{V}$, $V_{IH} = 2\text{V}$

Show SCIB project

- Where are input/output?
- What voltage levels are created?

FIFO queue analysis

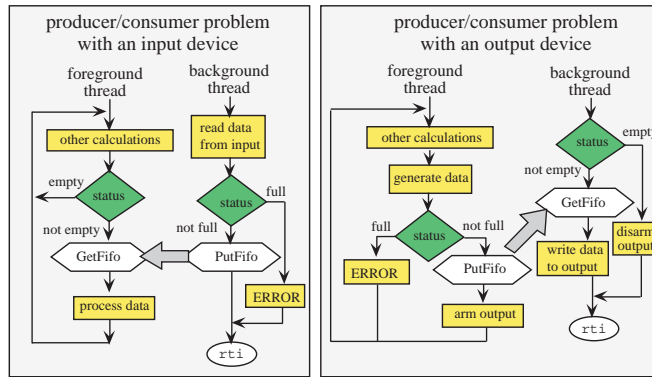


Figure 4.4. FIFO queues can be used to pass data between threads.

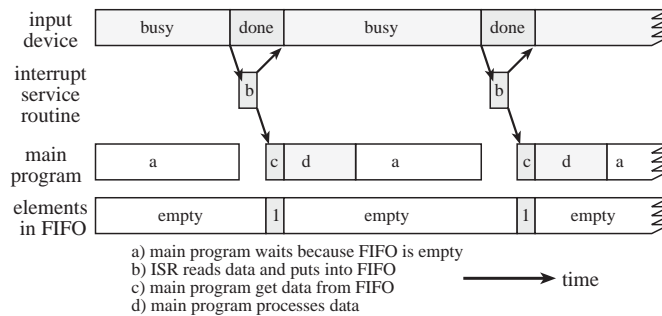


Figure 4.6. Hardware/software timing of an I/O bound input interface.

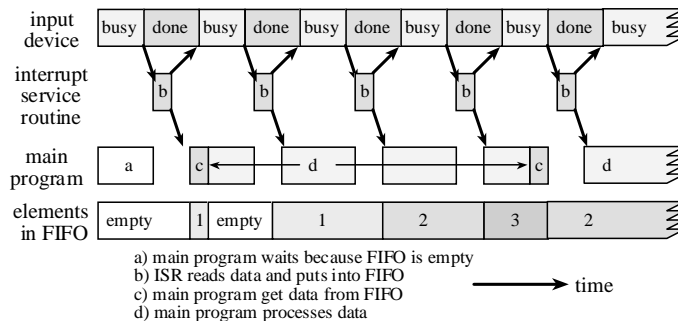


Figure 4.7. Hardware/software timing of an input interface during a high bandwidth burst.

Two causes of a FIFO full error

- 1) Average producer rate exceeds the average consumer rate
 - Sample ADC every 50 ms
 - Average time to process the sample is 51 ms
 - Solution: **decrease producer rate** or **increase consumer rate**
 - Lower sampling rate**
 - Faster computer**
 - More efficient compiler**
 - Rewrite time-critical code in assembly**
 - More computers (distributed processing)**
- 2) Producer rate temporarily exceeds the consumer rate
 - Sample ADC every 50 ms
 - Every 100th sample it takes 1 sec to process
 - Solution: **increase FIFO queue size**

It is very interesting to observe FIFO queue size during execution