

Jonathan W. Valvano First: _____ Last: _____

This is the closed book section. You must put your answers in the boxes on this answer page.
When you are done, you turn the closed-book part and pick up the open book part.

(4) Problem 1.
Choose A-F

(4) Problem 2.
Choose A-F

(4) Question 3.
Choose A-I

(4) Question 4.
ADC bits

(4) Question 5.
Choose A-F

(4) Question 6.
Choose A-F

(4) Question 7.
Choose A-F

(4) Question 8.
Choose A-F

(4) Question 9.
Choose A-F

(4) Question 10. Ethics Question

(4) Question 1. Consider the following interrupt service routine

```

unsigned short Elapsed; // time between interrupt
void interrupt 20 handler(void){
XXXXX unsigned short last=0;
    Elapsed = TCNT-last;
    last = TCNT;
}

```

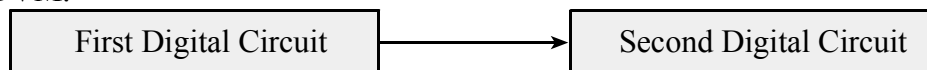
The goal is to measure the elapsed time from one interrupt call to the other. What qualifier do you place in the **XXXXX** position to make this measurement operational?

- A) **volatile** B) **float**
C) **static** D) **public**
E) **const** F) none (it is OK as it is)

(4) Question 2. Consider a system that needs to represent the numbers from 0.00 to 10.00 with a resolution of 0.01. No human output will be required. I.e., only calculations internal to the computer will be calculated and there are a lot of multiplies, divides, adds and subtracts with these numbers. Which number system would be most efficient on a microcontroller like the 9S12?

- A) Boolean B) Binary fixed-point
C) Decimal fixed-point D) Floating-point
E) Friendly F) Reentrant

(4) Question 3. Consider the situation in which the output of one digital circuit is connected to the input of another digital circuit. The difficulty arises because the two digital circuits are built with different logic families (e.g., 74LS, 74HC, 74S, etc.) There are no other connections on this signal, i.e., one output is tied to one input. The output specifications of the first circuit are V_{OH} , V_{OL} , I_{OH} and I_{OL} . The input specifications of the second circuit are V_{IH} , V_{IL} , I_{IH} and I_{IL} . These are the specifications, like you would find in a data sheet, not actual measurements of voltage and current like you would measure in lab with a DVM.

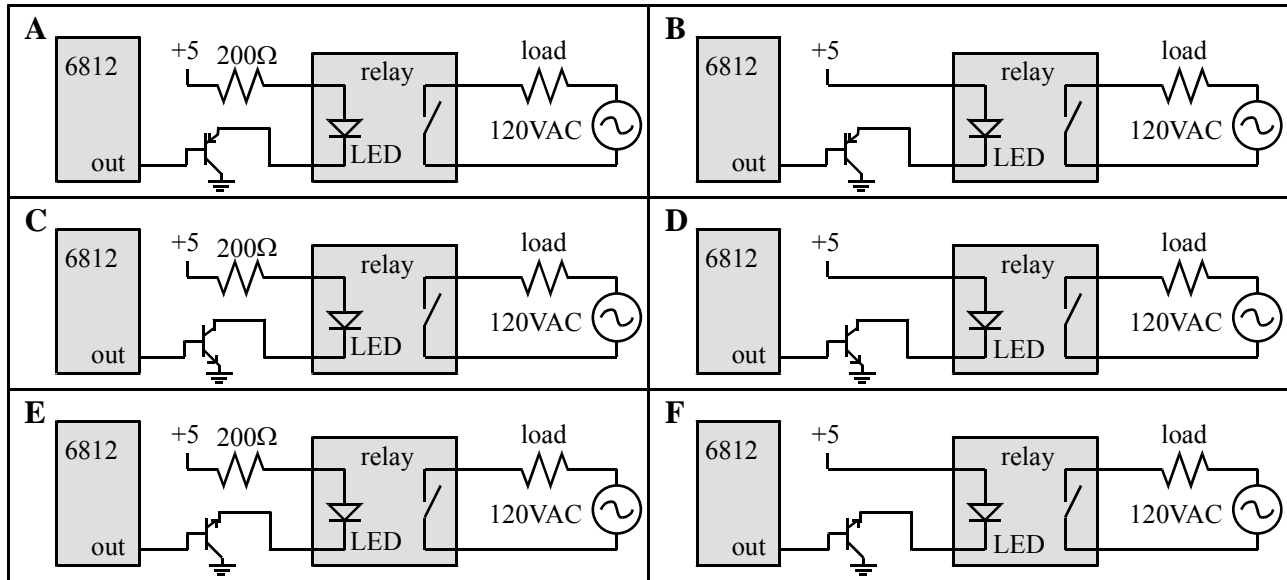


In a particular situation, you find that $V_{OH} \leq V_{IH}$ and currents are not an issue. Will it work? Secondly, if it doesn't work what is the simplest solution to make it work?

- A) Yes it will work. B) No, put a snubber diode to +5V
C) No, add a resistor to +5V D) No, put a capacitor to ground
E) No, add a resistor to ground F) No, add an op amp amplifier
G) No, add a capacitor to +5 H) No, add an instrumentation amplifier
H) No, add a 7406 driver I) No, add 2N2222 NPN transistor

(4) Question 4. The desired ADC range is -1V to +1V with a resolution of 0.001V. How many ADC bits are required?

(4) Question 5. A solid-state **relay** can be used to switch 120 VAC power to a load. For example, the load might be an AC motor. To activate the relay (apply power to the motor), you must energize an LED. The relay LED needs about 2V at 10 mA. To deactivate the relay, the relay coil current should be zero. Assume V_{CE} of the transistor is 0.5V. Which interface would you choose for this system. If more than one circuit works choose the best one.



(4) Question 6. What purpose might there be to use the PLL and slow down the 9S12?

- A) The system is CPU bound
- B) To make the batteries last longer on a battery-powered system
- C) In order to adjust the interrupt period when using RTI interrupts to a convenient value
- D) In order to balance the load between foreground and background threads
- E) To reduce latency
- F) None of the above, because there is never a reason to run slower

(4) Question 7. Consider the situation in which a FIFO queue is used to buffer data between a main program (e.g., `SCI_OutChar` that calls `TxFifo_Put`) and an output interrupt service routine (e.g., `SCIhandler` that calls `TxFifo_Get` and writes to `SCIDRL`). Experimental observations show this FIFO is usually empty, and at most 3 elements. What does it mean? Choose A-F.

- A) The system is CPU bound
- B) Bandwidth could be increased by increasing FIFO size
- C) The system is I/O bound
- D) The FIFO could be replaced by a global variable
- E) The latency is small and bounded
- F) Interrupts are not needed in this system

(4) **Question 8.** Consider the situation in which a FIFO queue is used to buffer data between an interrupt service routine (e.g., **SCIhandler** that reads **SCIDRL** and calls **RxFifo_Put**) and the main program (e.g., **SCI_InChar** that calls **RxFifo_Get**). Experimental observations show this FIFO is usually empty, and at most 3 elements. What does it mean? Choose A-F.

- A) The system is CPU bound
- B) Bandwidth could be increased by increasing FIFO size
- C) The system is I/O bound
- D) The FIFO could be replaced by a global variable
- E) The latency is small and bounded
- F) Interrupts are not needed in this system

(4) **Question 9.** This is a *functional debugging* question. However, the debugging instrument still needs to be *minimally intrusive*. Assume **y=Function(x)** is a function with 16-bit input **x** and 16-bit output **y** and is called from an ISR as part of a real-time system. The SCI, **PTT** and **PTAD** are unused by the system, and **PTT** and **PTAD** are digital outputs. The debugging code will be placed at the end just before the return, unless otherwise stated. **SCI_OutSDec** outputs a 16-bit signed integer. **BufX** and **BufY** are 16-bit signed global buffers of length 100, **n** is a global variable initialized to 0. Which debugging code would you add to verify the correctness of this function?

- A) **PTT=x; PTAD=y;**
- B) **SCI_OutSDec(x); SCI_OutSDec(y); // busy-wait**
- C) **SCI_OutSDec(x); SCI_OutSDec(y); // interrupt driven**
- D) **if(n<100){BufX[n]=x; BufY[n]=y; n++;}**
- E) **PTT |= 0x01; // at beginning**
PTT &= ~0x01; // at end
- D) **if(n<100){BufX[n]=x; BufY[n]=TCNT; n++;}**

(4) **Question 10.** Consider this situation. You are a new employee assigned to design a new feature for an existing product. During the testing of your feature, you discover a possible fault in another part of the system that might result in the compromise of safety. To whom do you first report this error?

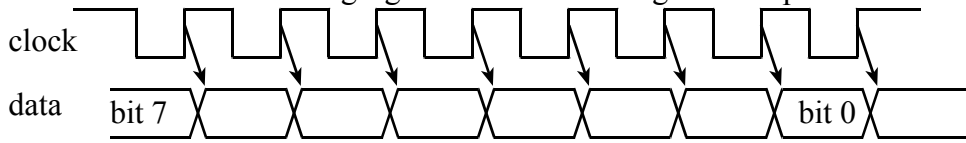
end of closed book section

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This is the open book section. You must put your answers on pages 5 to 8.

(5) Question 11. An SPI system is used to input data from an input device. The 9S12 is the master and the input device is a slave. The following figure shows the timing of the input device.



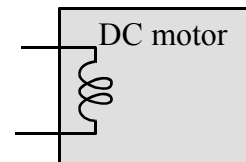
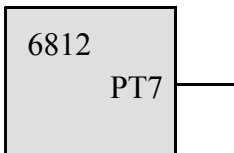
This clock comes from the 9S12 and this data is transmitted from the input device back to the 9S12. What is the appropriate configuration mode for **CPOL** and **CPHA** in the 9S12 master?

CPOL =

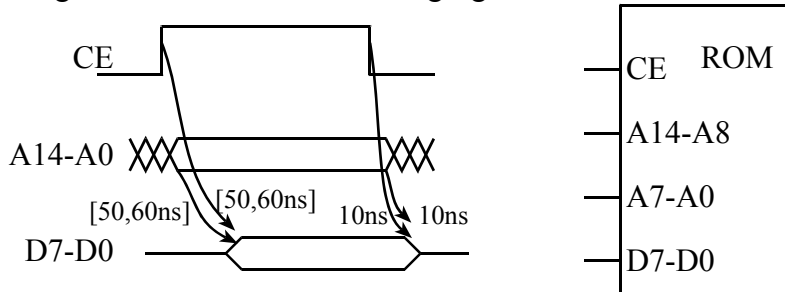
CPHA =

(10) Question 12. The goal of this question is to interface a DC motor. The software will output a digital low on PT7 to deactivate the motor (current = 0). To activate the motor you must deliver between 11 and 12V to the motor coil. The minimum resistance of the coil is 10 Ω (at maximum torque) and its inductance is 0.01 mH. Show the circuit diagram that interfaces PT7 to the motor. There are two power supplies to choose from +5V and +12V. Give part numbers and resistor values.

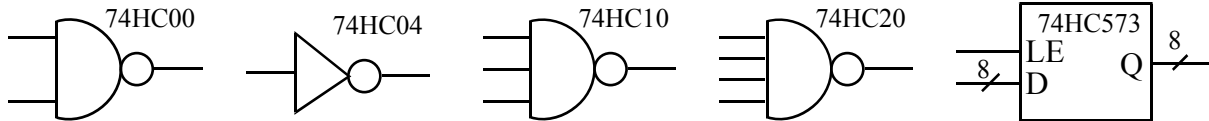
— +5V
 — +12V



(15) Question 13. Interface the following ROM to a 6811 running at 2 MHz. Assume the gate delay through each 74HC digital logic gate is [5ns min, 15ns max]. CE is positive logic. Assume there is no internal EEPROM or boot loader at BFxx. The full address decoder should select addresses \$8000 to \$FFFF. The ROM timing is described in the following figure:



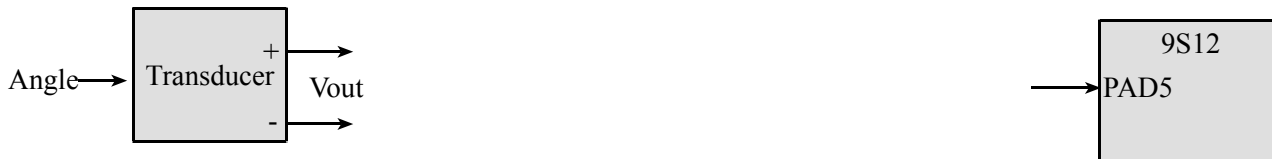
Part a) Design the interface between the ROM to the 6811. You are limited to the following digital devices (you can use more than one copy if you want)



Part b) Read data required is (450,510). Calculate the worst-case **Read Data Available** interval for this interface and show that the timing requirements are satisfied.

(15) Question 14. You will interface a transducer to the 9S12 needed for a data acquisition system to measure angle. The range of angles is 0 to 360°. The linear transducer has a sensitivity of 0.002778 V/degree. The angle signal exists in the 0 to 5 Hz frequency band.

Part a) The transducer output (V_{out}) is a differential voltage, with a range of 0 to 1V. The individual transducer output voltages are about 2.5V. A good CMRR is required. Design the analog circuit mapping the transducer output into the ADC input channel 5. (You do not have to add an antialiasing analog low pass filter.) Show chip numbers, resistor values, but not pin numbers.



Part b) Assuming the only error occurs in the 10-bit ADC, what decimal fixed-point resolution would you use (give units)?

Part c) Write a C function that converts the 10-bit ADC sample (0 to 1023) into the integer part of the fixed-point number representing angle. You do not need to call the ADC, just convert a 16-bit unsigned number ($0 \leq \text{rawData} \leq 1023$) to the integer part of the fixed-point angle.

```
unsigned short Convert(unsigned short rawData){
```

(15) Question 15. Assume PT0 is connected to a digital input that has a maximum frequency of 1000 Hz (high for at least 500 us, then low for at least 500us). The PS1 serial output is interfaced to another system. The serial protocol is 19200 bits/sec, 1 start, 8 data, and 1 stop bit. You may assume the E clock is 4 MHz (the PLL is not active). You will design the entire software system that outputs the letter 'V' (ASCII 0x56) to the SCI on every 5th rising edge of PT0. You must use input capture interrupts to detect the rising edges of PT0, and must use busy-wait synchronization for the SCI. The main program initializes the data structures, input capture, and SCI. Then the main program performs a "do nothing" while loop. An input capture interrupt occurs on each rising edge of PT0 and no backward jumps are allowed in the ISR. Other than the I/O port definitions no starter code is allowed.

```
#include <mc9s12c32.h>      /* derivative information */
```

Show all software required to make this system run.