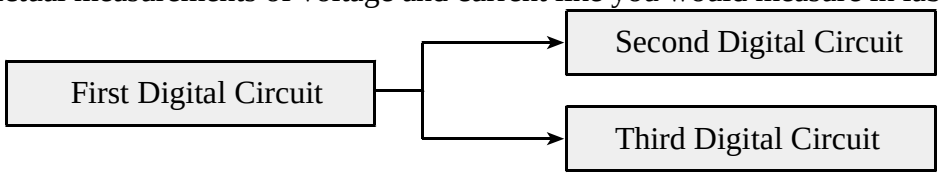
Jonathan W. Valvano First:_____ Last:_____

This is the closed book section. You must put your answers in the boxes on this answer page. When you are done, you turn in the closed-book part and can start the open book part.

Address	Bit 7	6	5	4	3	2	1	Bit 0	Name
$0082	ADPU	AFFC	ASWAI	ETRIGLE	ETRIGP	ETRIG	ASCIE	ASCIF	ATDCTL2
$0083	0	S8C	S4C	S2C	S1C	FIFO	FRZ1	FRZ0	ATDCTL3
$0084	SRES8	SMP1	SMP0	PRS4	PRS3	PRS2	PRS1	PRS0	ATDCTL4
$0085	DJM	DSGN	SCAN	MULT	0	CC	CB	CA	ATDCTL5
$0086	SCF	0	ETORF	FIFOR	0	CC2	CC1	CC0	ATDSTAT0
$008B	CCF7	CCF6	CCF5	CCF4	CCF3	CCF2	CCF1	CCF0	ATDSTAT1
$0090-1	Bit 15	14	13	12	11	10		Bit 0	ATDDR0
$0092-3	Bit 15	14	13	12	11	10		Bit 0	ATDDR1
$0094-5	Bit 15	14	13	12	11	10		Bit 0	ATDDR2
$0096-7	Bit 15	14	13	12	11	10		Bit 0	ATDDR3
$0098-9	Bit 15	14	13	12	11	10		Bit 0	ATDDR4
$009A-B	Bit 15	14	13	12	11	10		Bit 0	ATDDR5
$009C-D	Bit 15	14	13	12	11	10		Bit 0	ATDDR6
$009E-F	Bit 15	14	13	12	11	10		Bit 0	ATDDR7

(5) Question 1. Write a C function that samples ADC channel 4. Convert the 10-bit ADC sample to a fixed-point voltage with a resolution of 0.001V. For example, if the voltage on PAD4 is 1.234567V, return an integer somewhere in the range of 1230 to 1240. Assume the ADC is already initialized for a 10-bit sample, sequence length is 1, and the ADC clock is 2 MHz. Minimize errors due to dropout and overflow. Use busy-wait synchronization.

(5) Question 2. Consider the situation in which the output of one digital circuit is connected to the inputs of two other digital circuits. There are no other connections on this signal, i.e., one output is tied to two inputs. The output specifications of the first circuit are V_{OH}, V_{OL}, I_{OH} and I_{OL}. The input specifications of the second and third circuits are V_{IH}, V_{IL}, I_{IH} and I_{IL}. These are the specifications, like you would find in a data sheet, not actual measurements of voltage and current like you would measure in lab with a DVM.



Give the four **inequalities** relating these eight parameters that must be true in order for the interface to operate properly. It may be necessary to also add numbers to these inequalities.

V_{OH}	V_{IH}
V_{OL}	V_{IL}

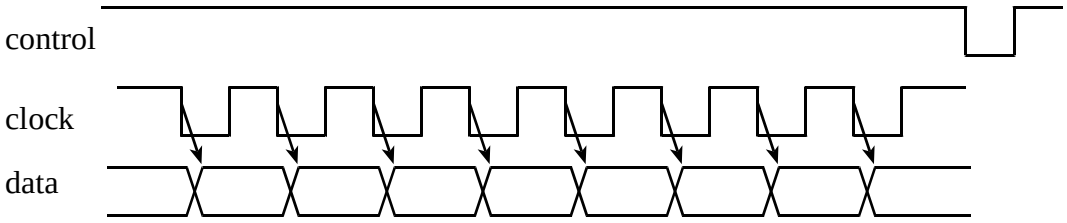
$\|I_{OH}\|$	$\|I_{IH}\|$
$\|I_{OL}\|$	$\|I_{IL}\|$

(5) Question 3. There are three input parameters: **`x0`**, **`x2`**, and **`y2`**, containing three 8-bit ADC samples. The sampling rate is 240 Hz. **`x0`** is the current 8-bit ADC sample, **`x2`** is the 8-bit ADC sample collected two times ago, and **`y2`** is the 8-bit output of the filter two times ago. Even though the parameters are defined as 16-bit signed integers, you may assume all four numbers are integers ranging from 0 to 255. There is an output parameter (**`y`**), which implements a high-Q 60 Hz digital notch filter. In other words, this equation will remove all 60 Hz components from the sampled data. All four variables are typed as **`short`**. Write C code to implement this digital filter without using floating point. Hint 0.78125 = 25/32, and 0.5625 = 18/32. Maximize for speed and minimize errors due to dropout and overflow. Just write C code to implement this equation, not the ADC sampling or the data structure that shifts the data.

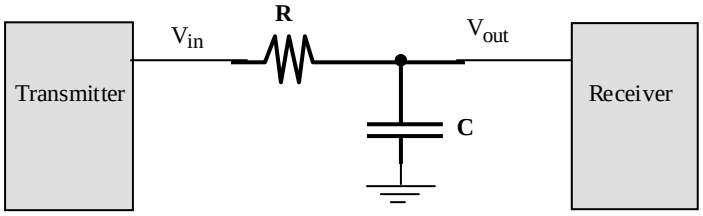
y = 0.78125*x0 + 0. 78125*x2 – 0.5625*y2

(5) Question 4. The control pin is interfaced to Port T bit 2, and the clock and data are connected to the SPI. The clock and data are created by the real SPI, and the control signal is bit-banged. On the 9S12C32 clock is SCK=PM5, and the data is MOSI=PM4. On the 9S12DP512 clock is SCK=PS6, the data is MOSI=PS5. Write a C function that outputs (transmits) one byte using the SPI port. You may assume the SPI is already initialized with the 9S12 as master, and PT2 is an output. Use busy-wait synchronization.

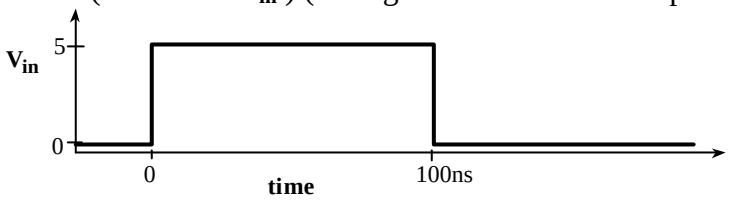
Address	Bit 7	6	5	4	3	2	1	Bit 0	Name
$00D8	SPIE	SPE	SPTIE	MSTR	CPOL	CPHA	SSOE	LSBF	SPICR1
$00D9	0	0	0	MODFEN	BIDIROE	0	SPISWAI	SPC0	SPICR2
$00DA	0	0	0	0	0	SPR2	SPR1	SPR0	SPIBR
$00DB	SPIF	0	SPTEF	MODF	0	0	0	0	SPISR
$00DD	Bit 7	6	5	4	3	2	1	Bit 0	SPIDR



(5) Question 5. This problem addresses the issue of capacitive loading on a high-speed serial transmission line like SPI. The SPI ports of two 9S12s are connected with a VERY long cable. We will model this cable as a single resistor in series with a capacitor, as shown in the figure below.



For this question, assume an ideal transmitter (output impedance of 0) and an ideal receiver (input impedance of infinity). Let **R** = 1 Ω, and **C** = 10 nF. Note that R*C is 10 ns. Consider a 5-V 100-ns pulse on the output of the transmitter (labeled as $\mathbf{V_{in}}$) (as might occur with a 5-Mbps SPI transmission)



Derive an equation for $\mathbf{V_{out}}$ as a function of time for the first 100 ns. Show your work and plug in for R*C equals 10 ns.

(5) Question 6. Consider this situation. You are a new employee assigned to test an existing product. During the testing of the device, you think you discover a possible fault in the system that might result in the compromise of safety. To whom do you first report this fault? Why?

(5) Question 7. The main program synthesizes a waveform (defines a sequence of DAC output values) and a periodic output compare interrupt will output the data to the DAC separated by a fixed time. A FIFO queue is used to buffer data between a main program (e.g., main program calls **`DAC_Out`**, which in turn calls **`Fifo_Put`**). An output compare interrupt service routine calls **`Fifo_Get`** and actually writes to the DAC. Experimental observations show this FIFO is usually empty, and has at most 3 elements. What does it mean? Choose A-F.

A) The system is CPU bound
B) Bandwidth could be increased by increasing FIFO size
C) The system is I/O bound
D) The FIFO could be replaced by a global variable
E) The latency is small and bounded _____
F) Interrupts are not needed in this system

(5) Question 8. RDRF interrupts are armed so that interrupts occur when new data arrives into the 9S12. Consider the situation in which a FIFO queue is used to buffer data between the RDRF ISR and the main program. The **`SCIhandler`** reads **`SCIDRL`** and saves the data by calling **`Fifo_Put`**. When the main program wants input it calls **`SCI_InChar`**, which in turn calls **`Fifo_Get`**. Experimental observations show this FIFO is usually empty, and has at most 3 elements. What does it mean? Choose A-F.

A) The system is CPU bound
B) Bandwidth could be increased by increasing FIFO size
C) The system is I/O bound
D) The FIFO could be replaced by a global variable
E) The latency is small and bounded _____
F) Interrupts are not needed in this system

(5) Problem 9. Consider the following input capture interrupting system with its corresponding assembly listing generated by the Metrowerks compiler. Assume the compiler initializes the permanently allocated variables to zero before executing **`main`**. The falling edge inputs on PT3 and PT2 can occur at any time, including at the same time. The object is to count the number of each type of interrupt.

```
void main(void) {
  DDRT &=~0x0C;  // PT3,PT2 are inputs
  TSCR1 = 0x80;  // enable TCNT
  TIOS &= ~0x0C; // PT3-2 input capture
  TCTL4 = 0xA0;  // falling edge
  TIE |= 0x0C;   // Arm IC3, IC2
asm cli          // enable
  for(;;) {
  }
}
interrupt 11 void IC3Han(void){
unsigned short static Count;
  TFLG1 = 0x08;   // acknowledge
  Count++;
}
interrupt 10 void IC2Han(void){
unsigned short static Count;
  TFLG1 = 0x04;   // acknowledge
  Count++;
}
```

```
main
  4200 1d02420c     BCLR  DDRT,#12
  4204 c680         LDAB  #128
  4206 5b46         STAB  TSCR1
  4208 4d400c       BCLR  TIOS,#12
  420b 86a0         LDAA  #160
  420d 5a4b         STAA  TCTL4
  420f 4c4c0c       BSET  TIE,#12
  4212 10ef         CLI
  4214 20fe         BRA   *+0
IC3Han
  4216 c608         LDAB  #8
  4218 5b4e         STAB  TFLG1
  421a fe3800       LDX   Count.1
  421d 08           INX
  421e 7e3800       STX   Count.1
  4221 0b           RTI
IC2Han
  4222 c604         LDAB  #4
  4224 5b4e         STAB  TFLG1
  4226 fe3802       LDX   Count.2
  4229 08           INX
  422a 7e3802       STX   Count.2
  422d 0b           RTI
```

Notice machine code in the listing includes addresses as linked by the compiler.

How would best describe the usage of **`Count`** in this system?

A) This is a perfectly appropriate usage of **`Count`**, because there are two permanently allocated variables with private scope, such that each variable counts the number of interrupts for each ISR.
B) There is a critical section bug because of the read/modify/write access to a shared global.
C) Because both ISRs share the same **`Count`**, the system can not distinguish between an IC2 and an IC3 interrupt.
D) The main program does not initialize **`Count`**, so its value is indeterminate.
E) The acknowledge statements in the two ISRs are not friendly because they affect all 8 bits of TFLG1.
F) None of the above is true.

Choose a letter A to F. _____

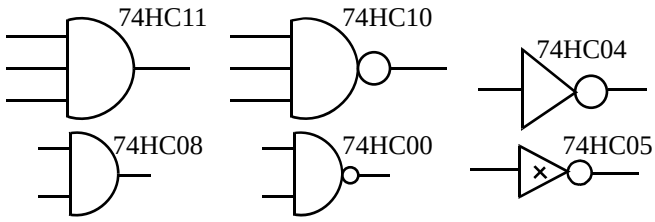
end of closed book section

Jonathan W. Valvano First:_____ Last:_____

Open book, open notes, calculator (no laptops, phones, devices with screens larger than a TI-89 calculator, devices with wireless communication). You must put your answers on these pages. Please don't turn in any extra sheets.

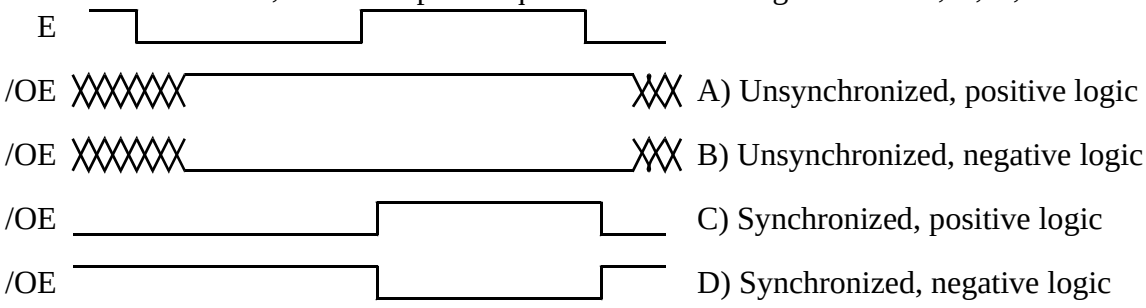
(20) Question 10. A 6811 system will be designed to provide for a latched input port. The latched input port contains 8 digital inputs (labeled 8D through 1D) and one input Clk. On the rising each of Clk, the inputs are clocked into the 74HC374. We will connect the Q outputs of a 74HC374 octal D flip-flip directly to the address/data bus of the 6811. This 8-bit latched input port will be placed at $A000, and respond only to read cycles. In particular, the /OE signal will be used to drive the input data onto the data bus during read cycles to $A000. Whenever the software reads from address $A000, it will get the data stored by the last rising edge of Clk. Write cycles to $A000 have no effect. The following is the memory map of the system

$0000 to $01FF 512 bytes of internal RAM
$1000 to $103F regular input/output ports
$2000 an 8-bit output port
$A000 this latched input port using a 74HC374
$B600 to $B7FF 512 bytes of EEPROM
$BF00 to $BFFF internal boot loader
$C000 to $FFFF external 16K EEPROM



Part a) Show the design of the address decoder for the latched input port. Give just the logic equation in this section, call the output of the decoder **Select**. The actual circuit will be shown in Part d)

Part b) Relative to the E clock, which shape is required for the /OE signal? Pick A, B, C, or D.



A) Unsynchronized, positive logic
B) Unsynchronized, negative logic
C) Synchronized, positive logic
D) Synchronized, negative logic

Part c) Show the design steps to create the 74HC374 **/OE** signal. Fill in this table

Select	R/W	E	/OE	action
0	0	0		
0	0	1		
0	1	0		
0	1	1		
1	0	0		
1	0	1		
1	1	0		
1	1	1		

Part d) Interface the 74HC374 to the 6811. Give chip numbers, but not pin numbers

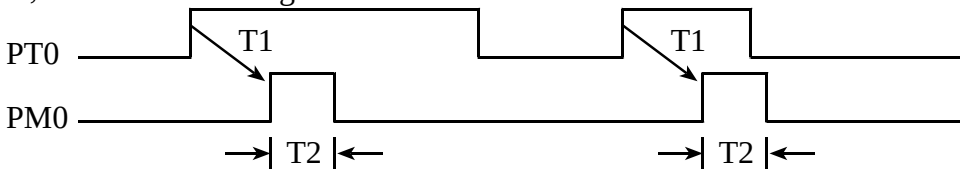
Part e) Assume the E clock is 2 MHz. This means RDR is (450,510). Assume the propagation delay for the 74HC04, 74HC05, 74HC08, 74HC10 and 74HC11 gates is [5,15ns], calculate the worst-case **Read Data Available** interval for this interface. The timing for the 74HC374 is given on the last page.

(10) Question 11. The input, V_{in}, is single-ended, not differential. Design an analog circuit with a transfer function of $V_{out} = 100*V_{in}-5$ using one rail to rail op amp powered by a single +5 V supply. You may use one REF03 2.50 V reference chip. The input range is 0.05 V to 0.10 V, and the output range is 0 to +5 V.

(5) Question 12. Assuming the frequency components of the input signal vary from DC (0 Hz) to 10 kHz, design and implement an appropriate analog filter for this signal. You may use one rail to rail op amp powered by a single +5 V supply. Show the design steps and specify all resistor and capacitor values.

(10) Question 13. Interface a 5 volt 5 amp DC motor to the 6812. The motor will spin when the software outputs a 1 to PT7, and it will stop spinning when the software outputs a 0 to PT7. Label all resistors, capacitors, inductors and diodes required. Please also label the part numbers on any transistors or op amps you use. Decide whether it is better to drive the motor from the +5 V or the +12 V supply.

(10) Question 14. PT0 is an input signal and PM0 is an output signal. Assume the E clock is 4 MHz. The goal is to use input capture 0 and output compare 1 interrupts to create a delayed pulse output, triggered on the rise of PT0, as shown in this figure:



T1 and T2 are time delays, given in μsec, as specified by two software global variables. Their initial values are given, but the system will allow the software to change these values dynamically. You may assume the period of the PT0 input is larger than T1+T2. You may also assume T1 and T2 are large compared to the software execution time.

```
unsigned short T1=1000;  // time in usec from rise of PT0 to rise of PM0
unsigned short T2=2000;  // time in usec from rise of PM0 to fall of PM0
```

Part a) Give the initialization code that sets PT0 as input, PM0 as output (initially zero). Activate, arm and enable input capture 0 and output compare 1 as needed. The main program will call this initialization once, then perform other unrelated tasks.

Part b) Show the input capture 0 interrupt service routine. No backward jumps allowed.

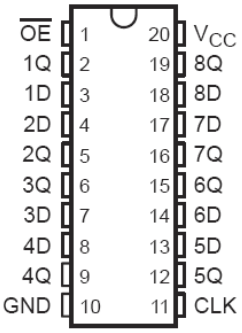
Part c) Show the output compare 1 interrupt service routine. No backward jumps allowed.

SN54HC374, SN74HC374
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

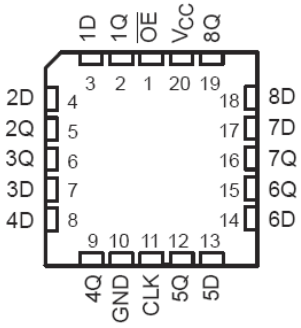
SCLS141E – DECEMBER 1982 – REVISED AUGUST 2003

- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State True Outputs Can Drive Up To 15 LSTTL Loads
- Eight D-Type Flip-Flops in a Single Package
- Full Parallel Access for Loading
- Low Power Consumption, 80-μA Max I_{CC}
- Typical t_{pd} = 14 ns
- ±6-mA Output Drive at 5 V
- Low Input Current of 1 μA Max

SN54HC374 . . . J OR W PACKAGE
SN74HC374 . . . DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC374 . . . FK PACKAGE
(TOP VIEW)



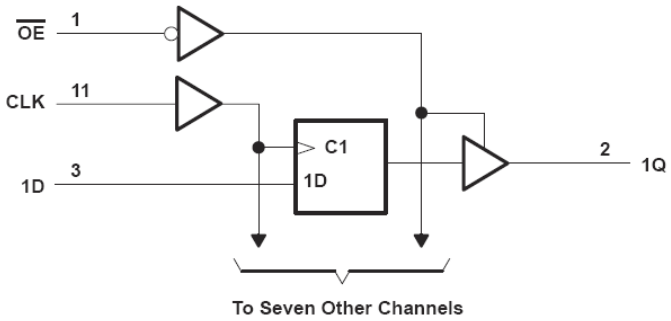
$\overline{OE}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic diagram (positive logic)



You may assume the setup time is 30ns and the hold time is 5ns relative to the rising edge of CLK. The time from /OE becoming 0 to Q output valid is 25 ns. The time from /OE becoming 1 to Q output not valid is 10 ns.