Jonathan W. Valvano First:_________________ Last:_____________________

This is the closed book section. You must put your answers in the boxes on this answer page. When you are done, you turn in the closed-book part and can start the open book part. CPE 2.214

(4) Question 1. Select A,B,C,D,E,F	**(4) Question 8.** Select A,B,C,D,E,F
(4) Question 2. Number of stack bytes	**(4) Question 9a.** Smallest T1
(4) Question 3. Give two instructions	**(3) Question 9b.** Smallest T2
(3) Question 4. Select A,B,C,D,E,F	**(3) Question 9c.** Smallest T3
(3) Question 5. Select A,B,C,D,E,F	**(4) Question 10a.** Baud rate
(3) Question 6. Select A,B,C,D,E,F	**(4) Question 10b.** Data transferred
(3) Question 7. Select A,B,C,D,E,F	**(4) Question 11.** Select A,B,C,D,E,F

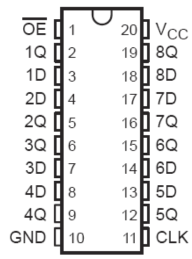
(5) Question 12. The first point of the IEEE Code of Ethics is *to accept responsibility in making engineering decisions consistent with the safety, health and welfare of the public, and to disclose promptly factors that might endanger the public or the environment;* Give one specific example of how this might apply to embedded systems.

SN54HC374, SN74HC374
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

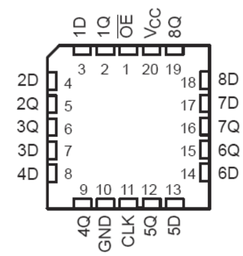
SCLS141E − DECEMBER 1982 − REVISED AUGUST 2003

- **Wide Operating Voltage Range of 2 V to 6 V**
- **High-Current 3-State True Outputs Can Drive Up To 15 LSTTL Loads**
- **Eight D-Type Flip-Flops in a Single Package**
- **Full Parallel Access for Loading**
- **Low Power Consumption, 80-µA Max I_{CC}**
- **Typical t_{pd} = 14 ns**
- **±6-mA Output Drive at 5 V**
- **Low Input Current of 1 µA Max**

SN54HC374 . . . J OR W PACKAGE
SN74HC374 . . . DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC374 . . . FK PACKAGE
(TOP VIEW)



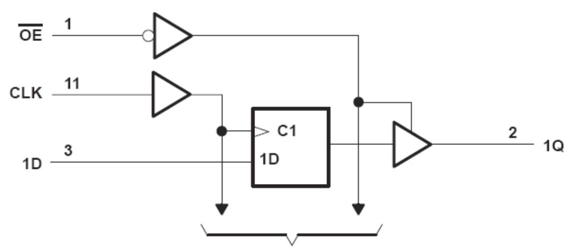
$\overline{OE}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE
(each flip-flop)

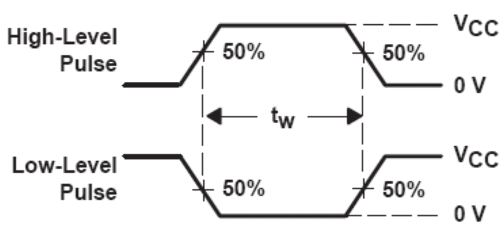
INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic diagram (positive logic)

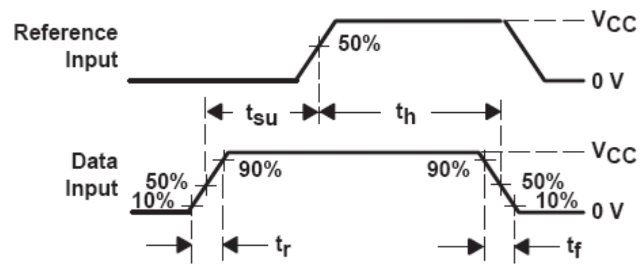


		V_{CC}	T_A = 25°C MIN	T_A = 25°C MAX	SN54HC374 MIN	SN54HC374 MAX	SN74HC374 MIN	SN74HC374 MAX	UNIT
f_{clock}	Clock frequency	2 V		6		4		5	MHz
		4.5 V		30		20		24	
		6 V		35		24		28	
t_w	Pulse duration, CLK high or low	2 V	80		120		100		ns
		4.5 V	16		24		20		
		6 V	14		20		17		
t_{su}	Setup time, data before CLK↑	2 V	100		150		125		ns
		4.5 V	20		30		25		
		6 V	17		25		21		
t_h	Hold time, data after CLK↑	2 V	10		13		12		ns
		4.5 V	5		5		5		
		6 V	5		5		5		

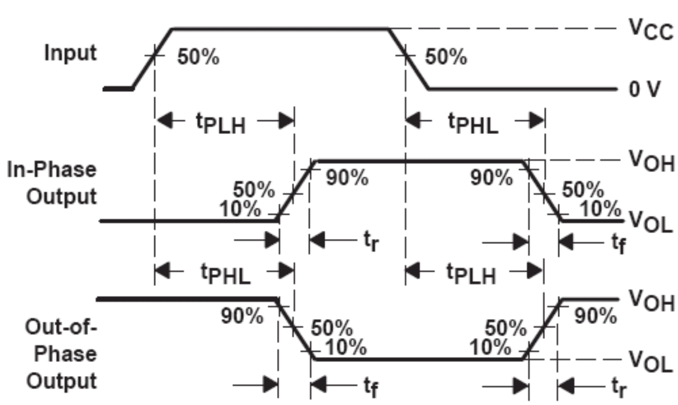
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25°C$ MIN	TYP	MAX	SN54HC374 MIN	MAX	SN74HC374 MIN	MAX	UNIT
f_{max}			2 V	6	12		4		5		MHz
			4.5 V	30	60		20		24		
			6 V	35	70		24		28		
t_{pd}	CLK	Any Q	2 V		63	180		270		225	ns
			4.5 V		17	36		54		45	
			6 V		15	31		46		38	
t_{en}	$\overline{OE}$	Any Q	2 V		60	150		225		190	ns
			4.5 V		16	30		45		38	
			6 V		14	26		38		32	
t_{dis}	$\overline{OE}$	Any Q	2 V		36	150		225		190	ns
			4.5 V		17	30		45		38	
			6 V		16	26		38		32	
t_t		Any Q	2 V		28	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	



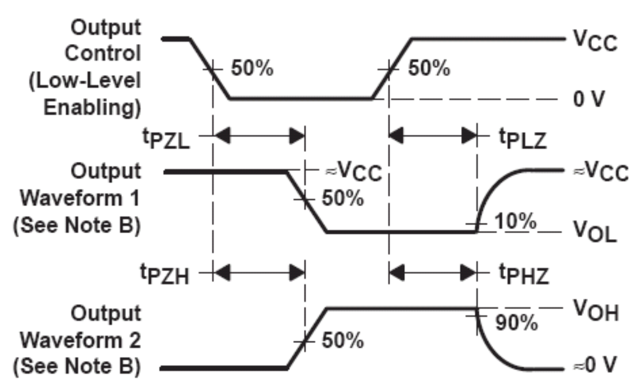
VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES FOR 3-STATE OUTPUTS

NOTES:
- A. C_L includes probe and test-fixture capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O = 50\ \Omega$, $t_r = 6$ ns, $t_f = 6$ ns.
- D. For clock inputs, f_{max} is measured when the input duty cycle is 50%.
- E. The outputs are measured one at a time with one input transition per measurement.
- F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- G. t_{PZL} and t_{PZH} are the same as t_{en}.
- H. t_{PLH} and t_{PHL} are the same as t_{pd}.

(4) Question 1. What fundamental electrical property is used to transfer digital data from one computer to another wirelessly.

A) Voltage B) Frequency
C) Current D) Phase
E) Energy F) Wavelength

Consider the following RTI interrupting system with its corresponding assembly code generated by a compiler (not Metrowerks). The listing includes absolute addresses. There are three permanently allocated variables: `Num` is at $0800, `Result` is at $0801 and `q` is at $0802. All three of these variables are initialized to 0 at start up, before `main` is called.

```
char Num,Result;

char LowPassFilter(const char n){
static char q=0;
  q = (n+q)/2;
  return q;
}

// called every 1.024 ms
void interrupt 7 handler(){
  CRGFLG = 0x80;
  Num++;
  Result = LowPassFilter(Num);
}

void main(void){char out;
  char p=0;
  CRGINT = 0x80;  // Arm RTI
  RTICTL = 0x33;  // 1.024ms
  asm cli
  for(;;) {
    out = LowPassFilter(p);
  }
}
```

```
$0800                    org $0800
$0800              Num    rmb 1
$0801              Result rmb 1
$0802              q      rmb 1
$4000                 org $4000
$4000              LowPassFilter:
$4000 B716            SEX   B,Y   ;n
$4002 F60802          LDAB  q
$4005 B714            SEX   B,D
$4007 19EE            LEAY  D,Y   ;n+q
$4009 B764            TFR   Y,D
$400B 47              ASRA
$400C 56              RORB      ;(n+q)/2
$400D 7B0802          STAB  q
$4010 3D              RTS
$4011              handler:
$4011 C680            LDAB  #128
$4013 5B37            STAB  CRGFLG
$4015 720800          INC   Num
$4018 F60800          LDAB  Num
$401B 07E3            BSR   LowPassFilter
$401D 7B0801          STAB  Result
$4020 0B              RTI
$4021              main:
$4021 36              PSHA           ;out
$4022 1808AF00        MOVB  #0,1,-SP ;p
$4026 CC3380          LDD   #13184
$4029 5B38            STAB  CRGINT
$402B 5A3B            STAA  RTICTL
$402D 10EF            CLI
$402F              loop:
$402F E680            LDAB  0,SP  ;p
$4031 07CD            BSR   LowPassFilter
$4033 6B81            STAB  1,SP  ;out
$4035 20F8            BRA   loop
$4037              begin:
$4037 CF4000          lds   #$4000
$403A 790800          clr   Num
$403D 790801          clr   Result
$4040 790802          clr   m
$4043 07DC            bsr   main
$4045 183E            stop
$FFF0                 org   $FFF0
$FFF0 4011            fdb   handler
$FFFE                 org   $FFFE
$FFFE 4037            fdb   begin
```

(4) Problem 2. The **lds** instruction at **start** will clear the stack. This is all the software. Calculate the maximum number of bytes that will be pushed on the stack at any given point as this system executes.

(4) Problem 3. There is a critical section in the software system shown above. State the exact two assembly instructions between which the critical section exists.

(3) Question 4. How is the parameter **n** passed into the function? Not in general, but in this system?

A) Reg A B) On the stack
C) Reg B D) In memory location $0800
E) Reg D F) The compiler optimized this so much the parameter was removed

(3) Question 5. Where is the variable **out** allocated in the main program?

A) Reg A B) On the stack
C) Reg B D) In memory location $0800
E) Reg D F) The compiler optimized this so much the parameter was removed

(3) Question 6. What does the **const** qualifier in the function **LowPassFilter()** mean?

A) private in scope B) the value is fixed and can not be changed by the function
C) stored in ROM D) tells the compiler to fetch a new value, and do not optimize
E) stored in global RAM F) promoted to the next high precision

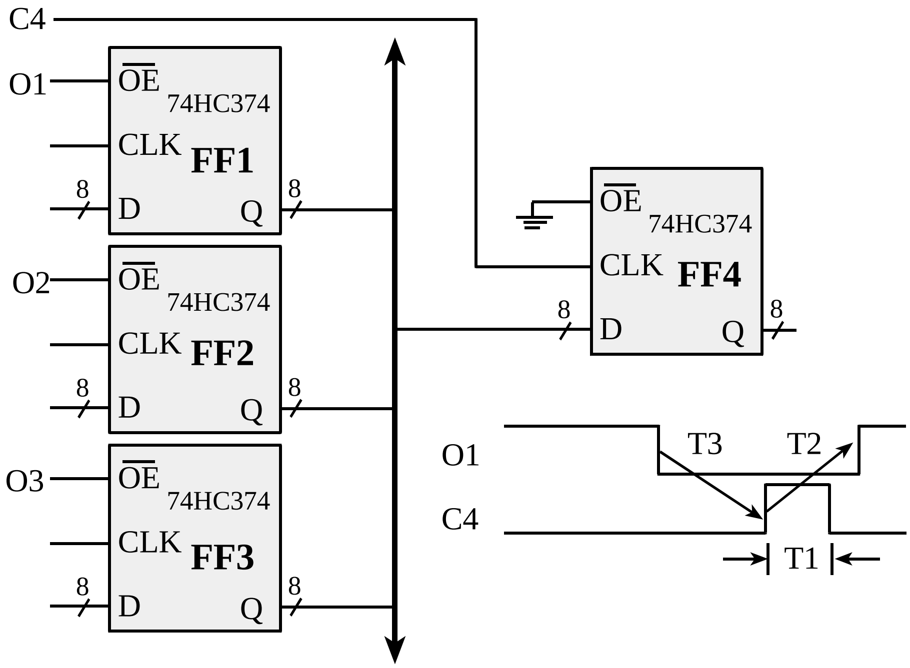
(3) Question 7. What does the **static** qualifier in the function **LowPassFilter()** mean?

A) public in scope B) the value is fixed and can not be changed by the function
C) stored in ROM D) stored in permanent RAM
D) promoted F) tells the compiler to fetch a new value, and do not optimize

(4) Question 8. LowPassFilter() is called from an ISR as part of a real-time system. The SCI, and **PTT** are unused by the system, and all **PTT** pins are digital outputs. The debugging code will be placed at the end just before the return, unless otherwise stated. **SCI_OutSDec8** outputs five ASCII characters as an 8-bit signed integer at 9600 bits/sec. **Bufq** and **Bufn** are global buffers of length 100 bytes, **i** is a global variable initialized to 0. Which code would you add to perform functional debugging of this real-time system?

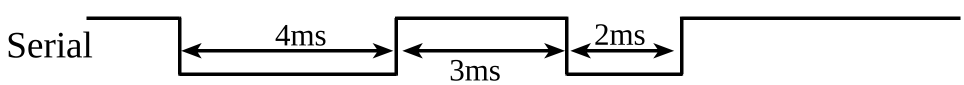
A)
```
PTT = q;
```
B)
```
asm sei
if(i<100){Bufq[i]=q; Bufn[i]=n; i++;}
asm cli
```
C)
```
asm sei
SCI_OutSDec8(q); SCI_OutSDec8(n);  // busy-wait
asm cli
```
D)
```
asm sei
SCI_OutSDec8(q); SCI_OutSDec8(n);  // interrupt driven
asm cli
```
E)
```
PTT |= 0x01;    // at beginning
PTT &= ~0x01;   // at end
```
F)
```
PTT ^= 0x01;    // at beginning
PTT ^= 0x02;    // at end
```

(10) Question 9. The goal of this system is to allow data to be transferred from one of the flip flops FF1 FF2 FF3 to the flip flop FF4. In this particular question we will be transferring data from FF1 to FF4. In this question we will not be considering the CLK and data inputs on flip flops FF1 FF2 FF3. I.e., assume the clock inputs on the flip flops FF1 FF2 FF3 have risen and valid data loaded into the internal Q values. When O1 goes low, the data from the internal Q on FF1 is driven out on the bus. When C4 rises, that same data is clocked into FF4. Use the 74HC374 parameters with 4.5V supply.



(3) Part a) What is the smallest **T1** time that can be reliably used?
(4) Part b) What is the smallest **T2** time that can be reliably used?
(3) Part c) What is the smallest **T3** time that can be reliably used?

(8) Question 10. The following waveform was measured on a PS0 serial input, which we think is one frame, but it might be two frames. The serial format is 1-start, 8-bit, and 1-stop bit.



(4) Part a) What is the baud rate?

(4) Part b) What data is being transferred?

(4) Question 11. A digital signal is interfaced to a microcontroller input. What happens to this digital interface when the effective capacitance to ground is increased?

A) no change	B) the signal to noise ratio improves
C) increase in DC current	D) the bandwidth decreases
E) decrease in DC current	F) causes a potential back emf pulse solved by a snubber diode

end of closed book section

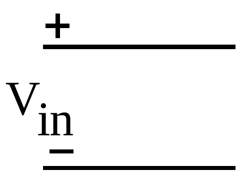
Jonathan W. Valvano First:_________________ Last:_____________________

Open book, open notes, calculator (no laptops, phones, devices with screens larger than a TI-89 calculator, devices with wireless communication). You must put your answers on these pages. Please don't turn in any extra sheets.

(5) Question 13. You are given a serial channel using a 100 kHz carrier frequency. The signal to noise ratio is 40 dB (10*log(10000) = 40). What is the maximum possible channel capacity in bits/sec.

(15) Question 14. There is a digital signal connected to PT4. Write software to measure the number of rising edges on that signal. Show the ritual function and the input capture ISR.

(10) Question 15. The input, V_{in}, is differential, not single-ended. Design an analog circuit with a transfer function of $V_{out} = 50*V_{in}+2.5$ powered by a single +5 V supply. You may use any of the analog chips we used in class or in lab. For example, you may use the REF03 2.50 V reference chip. The input range is -0.05 V to +0.05 V, and the output range is 0 to +5 V. Label all chips, resistors and capacitors as needed.



(15) Question 16. Interface QEE113 IR LED to the 9S12. Use PT5 and output compare interrupts to create a 20 kHz modulated output, 50% duty cycle. The period of PT5 should be 50 µs. There are three public functions: **`Init()`** **`On()`** and **`Off()`**. The user will call **`Init`** once at the beginning. The IR light is initially off. If the user calls **`On`**, then a 20 kHz IR light will be emitted using output compare 5 interrupts. If the user calls **`Off`**, the OC5 interrupts are disarmed and the light is turned off. Assume the E clock is 8 MHz.

Part a) Show the hardware interface. Label all chips, resistors and capacitors as needed.

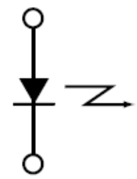
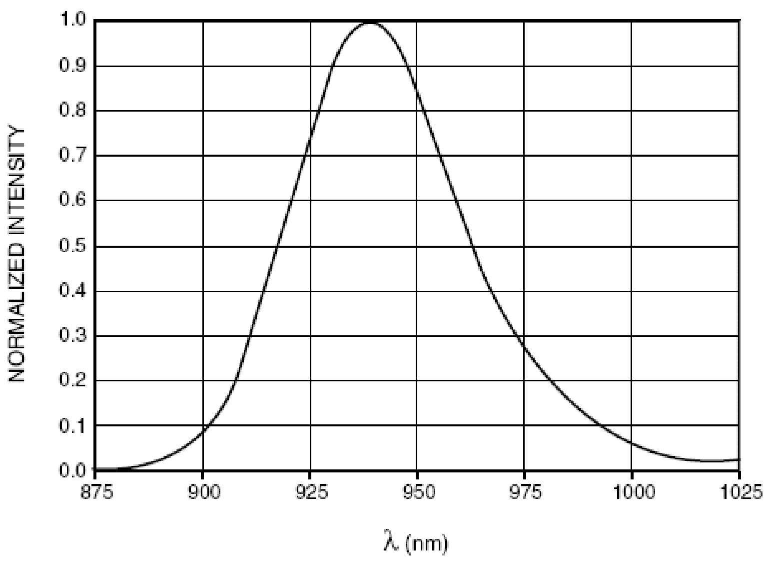
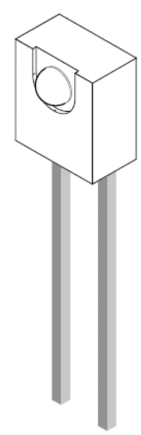


Fig. 4 Normalized Intensity vs. Wavelength





ELECTRICAL / OPTICAL CHARACTERISTICS (T_A =25°C)						
Parameter	**Test Conditions**	**Symbol**	**Min**	**Typ**	**Max**	**Units**
Peak Emission Wavelength	I_F = 100 mA	λ_{PE}	—	940	—	nm
Emission Angle	I_F = 100 mA	2Θ1/2	—	50	—	Deg.
Forward Voltage	I_F = 100 mA, tp = 20 ms	V_F	—	—	1.5	V
Reverse Current	V_R = 5 V	I_R	—	—	10	µA
Radiant Intensity	I_F = 100 mA, tp = 20 ms	I_E	3	—	12	mW/sr
Rise Time	I_F = 100 mA	t_r	—	1000	—	ns
Fall Time		t_f	—	1000	—	ns

Part b) Show the software including the three functions and the OC5 ISR

Part c) Will the IR LED actually emit light at 20 kHz? Prove it.