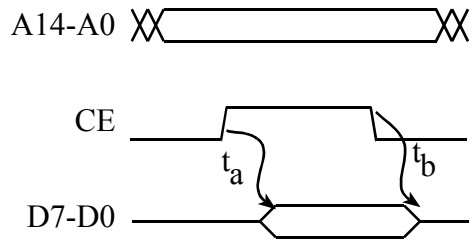
EE345L Spring 2005 Final



(8) Question 31. Design the interface between a 32k by 8-bit PROM and a 6811 running at 2 MHz. Implement full address decoding for addresses $8000-$FFFF. Assume t_a = 100 ns, and t_b = 20ns. Assume a 10ns gate delay through any digital logic and the 74HC573 address latch. The PROM has one control signal, CE, which when high reads data at the 15-bit address. Show just the circuit including chip numbers, but not pin numbers. The timing analysis is not required for this question.

(8) Question 31. Design the interface between a 32k by 8 bit PROM and a 6811
Step 1. Design the address decoder
$8000-$FFFF is 1xxx,xxxx,xxxx,xxxx
For fully decoded, specify all 0s and 1s. Select = A15 in positive logic
Step 2. Create a status table. The status table always starts like this

Select	R/W	Control Signals	Explanation
0	0		write cycle to another device
0	1		read cycle from another device
1	0		write cycle to our device
1	1		read cycle from our device

In this situation there is one control signal called CE

Select	R/W	CE	Explanation
0	0		write cycle to another device
0	1		read cycle from another device
1	0		write cycle to our device
1	1		read cycle from our device

Basically in the status table you make the memory do the necessary functions. In this case we want to turn off the device if the cycle is accesses another device. We will also turn it off if a write cycle occurs.

Select	R/W	CE	Explanation
0	0	**0**	write cycle to another device
0	1	**0**	read cycle from another device
1	0	**0**	write cycle to our device
1	1		read cycle from our device

Finally, we will activate it if there is a read cycle to our device

Select	R/W	CE	Explanation
0	0	0	write cycle to another device
0	1	0	read cycle from another device
1	0	0	write cycle to our device
1	1	**1**	read cycle from our device

Step 3. During the timing analysis we have to do two things. First, guarantee RDA overlaps RDR. And, second we have to make sure the memory doesn't drive the data bus

during the first half of the cycle (because the 6811 is driving the low address during the first half of the cycle. To prevent the memory data from colliding we will only drive data out of the memory when E=1. This is called synchronizing the read operation to E. To create a combined table, we expand the status table, adding the E as an input. The data from the status table in entered in the positions where E=1.

E	Select	R/W	CE	Explanation
0	0	0		
1	**0**	**0**	**0**	**write cycle to another device**
0	0	1		
1	**0**	**1**	**0**	**read cycle from another device**
0	0	0		
1	**1**	**0**	**0**	**write cycle to our device**
0	1	1		
1	**1**	**1**	**1**	**read cycle from our device**

To make the control signal low throughout the cycles when we wish to disable the memory, we place additional zeros

E	Select	R/W	CE	Explanation
0	0	0	**0**	
1	0	0	0	write cycle to another device
0	0	1	**0**	
1	0	1	0	read cycle from another device
0	0	0	**0**	
1	1	0	0	write cycle to our device
0	1	1		
1	1	1	1	read cycle from our device

To make the control signal synchronized positive logic, we place a 0,1 in those entries for the cycle we wish to activate. See the book Figure 9.28 and Table 9.9 for the choices that can be entered into the combined table.

E	Select	R/W	CE	Explanation
0	0	0	0	
1	0	0	0	write cycle to another device
0	0	1	0	
1	0	1	0	read cycle from another device
0	0	0	0	
1	1	0	0	write cycle to our device
0	1	1	**0**	
1	1	1	**1**	read cycle from our device

The question did not ask to verify timing, but if it did, we would write equations for RDA and RDR. The gate delay in this question is 10ns.

RDA = (rise of CE+t_a, fall of CE+t_b)

Because CE is synchronized to the E clock, the rise of CE will be 250+gate delay = 260. Similarly, the fall of CE will be 500+gate delay = 510. t_a = 100 ns, and t_b = 20ns

RDA = (260+100, 510+20) = (360,530)

RDR comes from the 6811. At 2 MHz it is

RDR = (450,510)

Notice that RDA overlaps RDR

Step 4. Develop the logic equation for the control signal and build it with real gates

CE = A15•R/W•E

Synchronized positive logic, activate PROM when R/W=1 and A15=1