Jonathan W. Valvano

You can use the textbook, but no other materials. You must put your answers in the boxes on the answer pages. You have 3 hours, so please allocate your time accordingly. ***Please read the entire quiz before starting.***

(4) Problem 1. Consider the following input capture interrupting system with its corresponding assembly code generated by the Metrowerks compiler. Assume at the time of the first instruction of **`main`**, there are exactly four (4) bytes pushed on the stack. In other words, after **`main`** executes **`BCLR`**, there will be 4 bytes on the stack. Calculate the maximum number of bytes that will be pushed on the stack at any given point as this system executes. This is all the software. The listing includes absolute addresses. The falling edge inputs on PT3 and PT2 can occur at any time, including at the same time.

```
void main(void) {
  DDRT &=~0x0C;  // PT3,PT2 are inputs
  TSCR1 = 0x80;  // enable TCNT
  TIOS &= ~0x0C; // PT3-2 input capture
  TCTL4 = 0xA0;  // falling edge
  TIE |= 0x0C;   // Arm IC3, IC2
asm cli          // enable
  for(;;) {
  }
}
interrupt 11 void IC3Han(void){
unsigned short static Count;
  TFLG1 = 0x08;   // acknowledge
  Count++;
}
interrupt 10 void IC2Han(void){
unsigned short static Count;
  TFLG1 = 0x04;   // acknowledge
  Count++;
}
```

```
main
  4200 1d02420c     BCLR  _DDRT,#12
  4204 c680         LDAB  #128
  4206 5b46         STAB  _TSCR1
  4208 4d400c       BCLR  _TIOS,#12
  420b 86a0         LDAA  #160
  420d 5a4b         STAA  _TCTL4
  420f 4c4c0c       BSET  _TIE,#12
  4212 10ef         CLI
  4214 20fe         BRA   *+0
IC3Han
  4216 c608         LDAB  #8
  4218 5b4e         STAB  _TFLG1
  421a fe3800       LDX   Count.1
  421d 08           INX
  421e 7e3800       STX   Count.1
  4221 0b           RTI
IC2Han
  4222 c604         LDAB  #4
  4224 5b4e         STAB  _TFLG1
  4226 fe3802       LDX   Count.2
  4229 08           INX
  422a 7e3802       STX   Count.2
  422d 0b           RTI
```

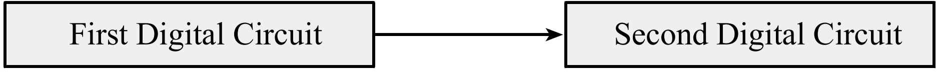
(4) Problem 2. Consider this **`Heap_Release`** function, which is part of a dynamic memory manager. The function exists at ROM locations $4110 to $411C, and the 16-bit **`FreePt`** is allocated in RAM at location $3852.

```
unsigned short static Heap[SIZE*NUM];
unsigned short static *FreePt;
void Heap_Release(unsigned short *pt){
unsigned short *oldFreePt;
  oldFreePt = FreePt;
  FreePt = pt;
  *pt = (unsigned short)oldFreePt;
}
```

```
Heap_Release
  4110 3b           PSHD
  4111 fc3852       LDD   FreePt
  4114 ee80         LDX   0,SP
  4116 7e3852       STX   FreePt
  4119 6c00         STD   0,X
  411b 3a           PULD
  411c 3d           RTS
```

Is there a critical section in the **`Heap_Release`** function? If so, specify the exact range of 16-bit hexadecimal addresses between which the critical section exists. For example, if you say there is a critical section between $4110 and $4114, then you are specifying an interrupt occurring between the **`PSHD`** and **`LDD`** instructions or between the **`LDD`** and **`LDX`** instructions could result in a corrupt heap, but interrupts occurring at other places in the function will be ok.

(8) Question 3. Consider the situation in which the output of one digital circuit is connected to the input of another digital circuit. The difficulty arises because the two digital circuits are built with different logic families (e.g., 74LS, 74HC, 74S, etc.) There are no other connections on this signal, i.e., one output is tied to one input. The output specifications of the first circuit are V_{OH}, V_{OL}, I_{OH} and I_{OL}. The input specifications of the second circuit are V_{IH}, V_{IL}, I_{IH} and I_{IL}. These are the specifications, like you would find in a data sheet, not actual measurements of voltage and current like you would measure in lab with a DVM. In order for this system to operate properly, choose the proper specifications.



(2) Part a) Consider the voltage when the digital signal is high. Which of these specifications must be satisfied?

A) $V_{OH} \geq V_{IH}$ **B)** $V_{OH} = V_{IH}$
C) $V_{OH} \leq V_{IH}$ **D)** It doesn't matter

(2) Part b) Consider the voltage when the digital signal is low. Which of these specifications must be satisfied?

A) $V_{OL} \geq V_{IL}$ **B)** $V_{OL} = V_{IL}$
C) $V_{OL}| \leq V_{IL}$ **D)** It doesn't matter

(2) Part c) Consider the current when the digital signal is high. Which of these specifications must be satisfied?

A) $|I_{OH}| \geq |I_{IH}|$ **B)** $|I_{OH}| = |I_{IH}|$
C) $|I_{OH}| \leq |I_{IH}|$ **D)** It doesn't matter

(2) Part d) Consider the current when the digital signal is low. Which of these specifications must be satisfied?

A) $|I_{OL}| \geq |I_{IL}|$ **B)** $|I_{OL}| = |I_{IL}|$
C) $|I_{OL}| \leq |I_{IL}|$ **D)** It doesn't matter

(4) Question 4. Why do we define I/O ports like `TCNT` as `volatile`? Choose A-F.

A) It is 16 bits wide.
B) It needs to be permanently allocated.
C) It is public.
D) It changes value by means other than the direct action of the software.
E) It is private.
F) The software is not allowed to change its value.

(4) Question 5. What purpose might there be to use the PLL and slow down the 6812?

A) The system is CPU bound
B) To make the batteries last longer on a battery-powered system
C) In order to adjust the interrupt period when using RTI interrupts to a convenient value
D) In order to balance the load between foreground and background threads
E) To reduce latency
F) None of the above, because there is never a reason to run slower

(4) Question 6. Consider the situation in which a FIFO queue is used to buffer data between a main program (e.g., `SCI_OutChar` that calls `TxFifo_Put`) and an output interrupt service routine (e.g., `SCIhandler` that calls `TxFifo_Get` and writes to `SCIDRL`). Experimental observations show this FIFO is usually empty, and at most 3 elements. What does it mean? Choose A-F.

A) The system is I/O bound
B) Bandwidth could be increased by increasing FIFO size
C) The system is CPU bound
D) The FIFO could be replaced by a global variable
E) The latency is small and bounded
F) Interrupts are not needed in this system

(4) Question 7. Consider the situation in which the interrupt-driven SCI device is used for debugging purposes. In other words, the basic system operation does not require SCI output, but the programmer adds calls to `SCI_OutUDec` in order to visualize strategic parameters in real-time during execution. Which statement best describes the intrusiveness of this debugging method?

A) If it is the case that the TxFifo becomes full, `SCI_OutUDec` will have to wait for the output to complete. In this situation, it is highly intrusive.
B) The TxFifo can always be made large enough so it never fills. Consequently, the time to execute `SCI_OutUDec` will be short. Therefore, this debugging method is always minimally intrusive.
C) It is nonintrusive, because the SCI is not required for basic system operations.
D) It can be made minimally intrusive if the baud rate is set at the maximum rate.
E) It is minimally intrusive because output occurs in the background.

(8) Question 8. Consider the situation in which 1) the ritual first executes, 2) an output compare interrupt 7 is requested, and then 3) the OC7 ISR executes. For each operation, which occurs first?

Part a) Consider the sequence order of interrupt enable and OC7 trigger. Which occurs first?

A) The ritual first executes `cli` enabling interrupts then the C7F flag will be set
B) C7F flag first is set by the timer hardware then the ritual executes `cli`
C) It is possible that C7F could be set before or after the ritual executes `cli`

Part b) During the context switch as the computer suspends the main thread and launches the interrupt thread, it disables interrupts and saves registers on the stack. Which occurs first?

A) The hardware first sets I=1 then CCR is pushed on the stack
B) CCR is first pushed on the stack then the hardware sets I=1
C) These events could happen in either order

Part c) The output compare ISR will both clear C7F and execute `rti`. Which occurs first?

A) ISR first executes `rti` then clears C7F
B) ISR first clears C7F then executes `rti`
C) Could happen in either order

Part d) In order to reduce latency of other interrupts, this ISR reenables interrupts. Which occurs first?

A) ISR first reenables interrupts executing `cli` then clears C7F
B) ISR first clears C7F then reenables interrupts executing `cli`
C) The ISR could execute `cli` and clear C7F in either order

(2) Question 9. Which of these code segments will acknowledge a SCI RDRF interrupt? Assume `data` is an 8-bit local variable. If there is more than one answer, choose the simplest.

A) `data = SCIDRL;` B) `SCIDRL = data;`
C) `TFLG1 = 0x20;` D) `if(SCISR1&0x20) data = SCIDRL;`
E) `SCISR1 = 0x20;` F) `SCISR1 &= ~0x20;`

(4) Question 10. A 9-bit ADC has an input range of 0 to +10V. What is the ADC precision with units?

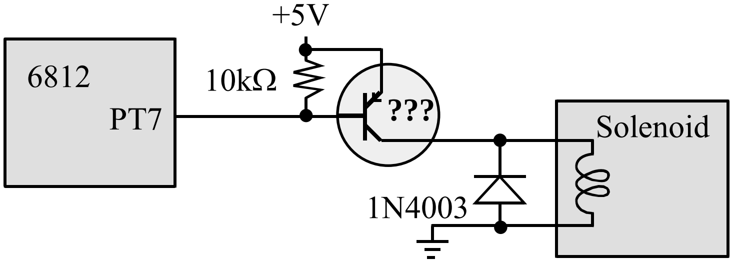
(6) Question 11. Assume there are three analog signals connected to PAD4, PAD3, and PAD2. The ADC will be used in 10-bit, right-justified, unsigned format.

Part a) The goal is to initialize the ADC so that one start command will sample exactly these three channels, no more no less. To what value should you initialize **`ATDCTL3`**? Give your answer in hex.

Part b) In order to start the ADC conversions of these three channels, what value should be written into **`ATDCTL5`**. Give your answer in hexadecimal.

Part c) After the three ADC conversions are finished, which I/O register contains the 10-bit result of the ADC conversion of channel PAD3? I.e., choose from **`ATDDR0`**, **`ATDDR1`**, … or **`ATDDR7`**.

(4) Question 12. A solenoid is used to lock and unlock a door. The software will output a digital low on PT7 to activate the solenoid (locking the door). For this situation, you must deliver between 4 to 5V to the solenoid electro-magnet (coil). To deactivate the solenoid (unlocking the door), the coil current should be zero. The resistance of the coil is 10 Ω and its inductance is 0.1 mH. Which transistor would you use between the 6812 and the solenoid coil?

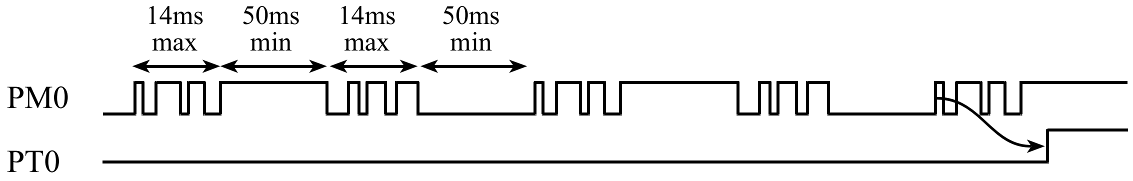


A) 2N2222
B) 2N2907
C) TIP120
D) TIP125
E) None is required, you can connect it directly

(2) Question 13. The ten points of the IEEE Code of Ethics are summarized as
1. to **accept responsibility** consistent with the **safety, health and welfare** of the public;
2. to **avoid** real or perceived **conflicts of interest** whenever possible, and to disclose them;
3. to be **honest and realistic** in stating claims or estimates based on available data;
4. to **reject bribery** in all its forms;
5. to **improve the understanding of technology**, its application, and consequences;
6. to **maintain and improve our technical competence**;
7. to **seek, accept, and offer honest criticism** of technical work, to acknowledge and correct errors;
8. to **treat fairly all persons**;
9. to **avoid injuring others**, their property, reputation, or employment **by false or malicious action**;
10. to **assist** colleagues and to **support them in following this code of ethics**.

Which of the ten points specifies it is important not only to test our devices, but also to clearly document the testing procedure?

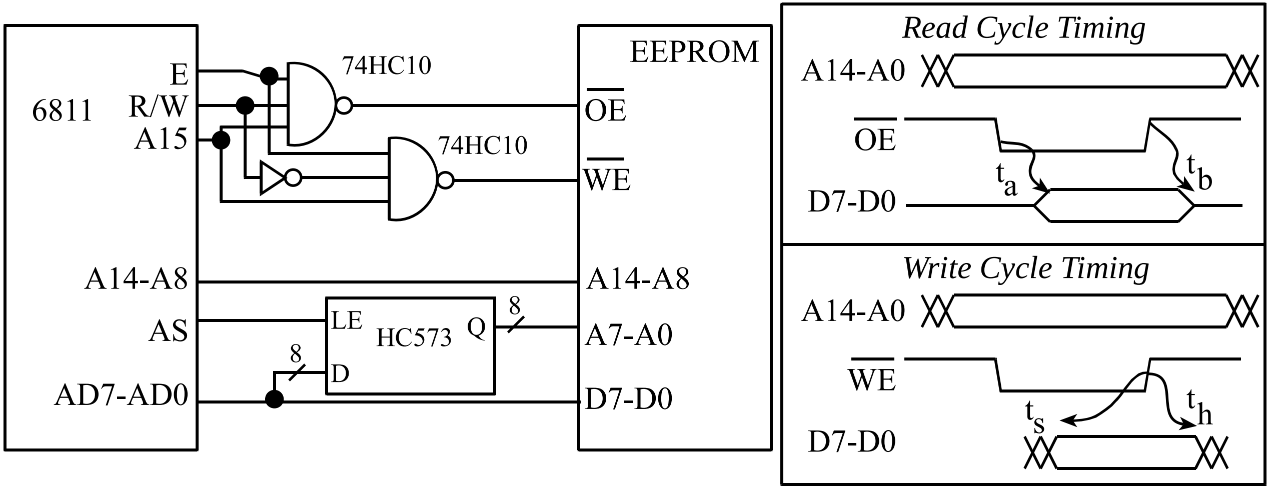
(6) Question 14. Consider a system with a positive logic switch connected to Port M bit 0. The input will be high if the switch is pressed, and the input will be low if the switch is not pressed. The switch bounces on touch and release. There is one LED connected to Port T bit 0. The LED is on if the software outputs a high, and the LED will be off if the software outputs a low. The LED should be initially off and the goal is to turn on the LED after the switch is pressed three times (i.e., touch, release, touch, release, touch). After the switch has been pressed 3 times the LED will remain on. The time delay between the third touch and the LED coming on can be any value less than 50ms. Draw a Moore FSM graph solving this problem with one input, one output and a time delay for each state. The execution order repeats the sequence: output, wait, input, next. Specify the initial state. For each state, please give a descriptive name, an output, a time to wait in ms, and input-dependent next states.



(6) Question 15. Design a minimal-cost positive-logic address decoder for **YourDevice** in the following system. Show the design steps, the logic equation and the digital circuit. You do not have to design all four address decoders, just the one for **YourDevice**. Specify chip numbers.

Ports	\$5800-\$58FF
RAM	\$D000-\$D3FF
YourDevice	\$D800-\$DFFF
ROM	\$E000-\$FFFF

(8) Question 16. This interface connects a 32k by 8-bit EEPROM to a 6811 running at 2 MHz. Assume the gate delay through each 74HC digital logic gate is [10ns min, 20ns max]. The full address decoder selects addresses \$8000 to \$FFFF. The EEPROM has two control signals, $\overline{OE}$ and $\overline{WE}$. During a read cycle $\overline{WE}$=1 and $\overline{OE}$=0, and during a write cycle, $\overline{WE}$=0 and $\overline{OE}$=1. $\mathbf{t_a}$ and $\mathbf{t_b}$ are the EEPROM read cycle timing parameters. $\mathbf{t_s}$ and $\mathbf{t_h}$ are the EEPROM write cycle timing parameters.



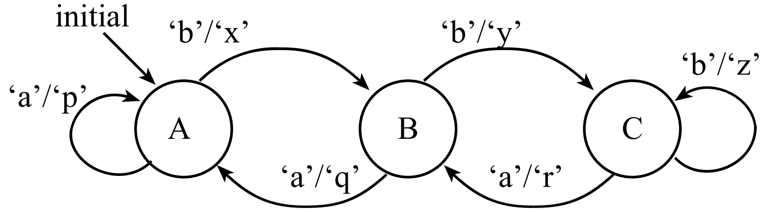
Part a) What is the largest value possible for $\mathbf{t_a}$ so that read data available overlaps read data required?
Part b) What is the largest value possible for $\mathbf{t_s}$ so that write data available overlaps write data required?

(6) Question 17. Let **x**, **y** be 16-bit unsigned binary fixed-point numbers with a resolution of 1/256. The corresponding integer parts are defined in global memory as

```
unsigned short Ix, Iy;
```

Write C code to implement **y = 0.6*x+2.0**

(16) Question 18. The overall objective of this problem is to design an interrupt driven finite state machine. The input/output occurs using the SCI serial interface.



The FSM graph shows there are two possible inputs ‘a’ and ‘b’. Any input other than ‘a’ and ‘b’ should be ignored. There are six possible outputs. Initially the system is in State A. From State A, if the input is ‘a’, then the output is ‘p’ and the system remains in State A. From State A, if the input is ‘b’, then the output is ‘x’ and the system switches to State B. You must use the following FSM data structure.

```
const struct State{
  unsigned char Out[2];         // outputs if input=‘a’ ‘b’
  const struct State *Next[2];  // Next state if input=‘a’ ‘b’
};
typedef const struct State StateType;
StateType *Pt;  // pointer to current state
#define SA &fsm[0]
#define SB &fsm[1]
#define SC &fsm[2]
StateType fsm[3]={
  {{‘p’,‘x’,{SA,SB}},
  {{‘q’,‘y’,{SA,SC}},
  {{‘r’,‘z’,{SA,SC}}
};
void main(void){
  FSM_Init();  // your solution to part a)
  while(1){  };
}
```

This FSM is the only I/O occurring on the SCI. Both the SCI transmit and receive channels should be active, but only RDRF should be armed. The RDRF interrupt service routine should execute the FSM in the background. Assume the M clock is 4 MHz. The SCI protocol is 1 start bit, 8-bit data, 1 stop bit and no parity. The baud rate is 9600 bits/sec. Other than the software shown above, you must write all the software required to run this FSM.

Part a) Show the initializing ritual. Once the ritual is executed, the FSM runs in the background and the main program is free to execute other unrelated tasks. See the above `main` program.

Part b) Show the SCI interrupt service routine. No backward jumps are allowed.

Jonathan W. Valvano First:_________________ Last:_____________________

(4) Problem 1. Give number		**(2) Question 8a**. Choose A,B,C	
(4) Problem 2. Critical section		**(2) Question 8b**. Choose A,B,C	
(2) Question 3a. Choose A,B,C		**(2) Question 8c**. Choose A,B,C	
(2) Question 3b. Choose A,B,C		**(2) Question 8d**. Choose A,B,C	
(2) Question 3c. Choose A,B,C		**(2) Question 9.** Choose A-F	
(2) Question 3d. Choose A,B,C		**(4) Question 10.** Precision (units)	
(4) Question 4. Choose A-F		**(2) Question 11a**. **ATDCTL3** value	
(4) Question 5. Choose A-F		**(2) Question 11b**. **ATDCTL5** value	
(4) Question 6. Choose A-F		**(2) Question 11c**. Specify register	
(4) Question 7. Choose A-E		**(4) Question 12.** Choose A-E	
		(2) Question 13. Choose 1-10	

(6) Question 14. Draw the FSM graph (no software or hardware, just the state graph)

(6) Question 15. Decoder with A15-A0 inputs and YourDeviceSelect as output (give chip numbers)

(4) Question 16a. Largest $\mathbf{t_a}$

(4) Question 16b. Largest $\mathbf{t_s}$

(6) Question 17. Write one line of C code

(16) Question 18.

(6) Part a) SCI ritual	(10) Part b) SCI interrupt service routine