

Last Name: _____ First Name: _____

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February 23, 2005, 1:00pm-1:05pm

Answer two of the following four questions, putting your answers in the boxes. The 6811 memory bus interfacing timing diagram is on the back. Assume a 2.0 MHz E clock. Two of the following questions **can not** be answered using just the 6811 data sheet. Answer two questions and leave the other two questions blank. **These are intervals in the form of (number1, number2).**

Question 1. Determine Read Data Available

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Question 2. Determine Read Data Required

$(t_1 - t_4 - t_{17}, t_1 + t_{18a}) = (450, 510)$
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Question 3. Determine Write Data Available

$(t_2 + t_4 + t_{19}, t_1 + t_{21}) = (378, 533)$

Question 4. Determine Write Data Required

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Rational for this question:

This timing diagram and table will be in this exact form on Quiz 1. You will need to know what RDA RDR WDA WDR mean, and how to find two of these from this timing diagram.

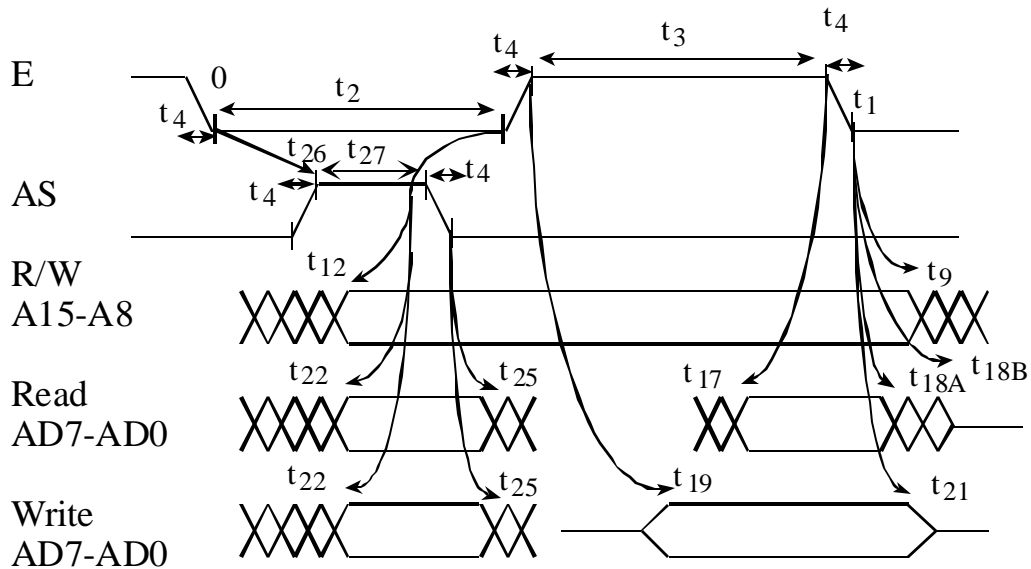


Figure 9.34. Simplified bus timing for the 6811 in expanded mode.

Num	Characteristic	1.0 MHz	2.0 MHz	2.1 MHz	Units
	Frequency	1.0	2.0	2.1	MHz
t₁	Cycle Time	1000	500	476	ns
t₂	Pulse Width E low	480	230	218	ns
t₃	Pulse Width E high	480	230	218	ns
t₄	rise/fall time	20	20	20	ns
t₉	address hold time	95.5 min	33 min	30 min	ns
t₁₂	A15-A8, R/W valid time	281.5 min	94 min	85 min	ns
t₁₇	Read data setup time	30 min	30 min	30 min	ns
t_{18A}	Read data hold time	10 min	10 min	10 min	ns
t_{18B}	Read data goes hiZ	145.5 max	83 max	80 max	ns
t₁₉	Write data delay time	190.5 max	128 max	125 max	ns
t₂₁	Write data hold time	95.5 min	33 min	30 min	ns
t₂₂	A7-A0 valid time	271.5 min	84 min	75 min	ns
t₂₅	A7-A0 hold time	95.5 min	33 min	30 min	ns
t₂₆	E to AS rise time	115.5	53	50	ns
t₂₇	AS pulse width	221	96	90	ns