

Last Name: \_\_\_\_\_ First Name: \_\_\_\_\_

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The goal is to create a periodic interrupt using output compare channel 0. For each of the following events, decide if

- A) this is software that is executed once in the initialization ritual
- B) this is the triggering event that will cause an OC0 interrupt to occur
- C) these hardware steps will occur automatically as the computer switches to the OC0 interrupt
- D) this is software that is executed every OC0 interrupt (the interrupt service routine)

event	Specify A,B,C, or D
TIOS  = 0x01; TMSK1  = 0x01; //MC68HC812A4 TIE  = 0x01; //9S12C32	A activate
rti pulls CCR,B,A,X,Y,PC	D return
asm cli	A enable
push PC,Y,X,A,B,CCR I=1 (disable) PC = [FFEE] (address of OC0han)	C context switch
TFLG1 = 0x01;	D acknowledge
TC0 = TCNT+50;	A when first
COF=1, set when TCNT equals TC0	B trigger
TSCR = 0x80; //MC68HC812A4 TSCR1= 0x80; //9S12C32	A turn on
TMSK2= 0x33; //MC68HC812A4 TSCR2= 0x03; PACTL = 0; //9S12C32	A set TCNT rate
TC0 = TC0+10000;	D set OC0 period

**Common Registers, TCNT, TC0 and**

**TIOS**

	Bit 7	6	5	4	3	2	1	Bit 0
R	IOS7	IOS6	IOS5	IOS4	IOS3	IOS2	IOS1	IOS0
W								
RESET:	0	0	0	0	0	0	0	0

IOS[7:0] — Input Capture or Output Compare Channel Configuration  
 1 = The corresponding channel acts as an output compare.  
 0 = The corresponding channel acts as an input capture.

**TFLG1**

	Bit 7	6	5	4	3	2	1	Bit 0
R	C7F	C6F	C5F	C4F	C3F	C2F	C1F	C0F
W								
RESET:	0	0	0	0	0	0	0	0

These flags are set when an input capture or output compare event occurs. Clear a channel flag by writing one to it.

**TMKS2  
TIE**

	Bit 7	6	5	4	3	2	1	Bit 0
R	C7I	C6I	C5I	C4I	C3I	C2I	C1I	C0I
W								
RESET:	0	0	0	0	0	0	0	0

C7I-C0I — Input Capture/Output Compare "x" Interrupt Enable.

**TSCR  
TSCR1**

	Bit 7	6	5	4	3	2	1	Bit 0
R	TEN	TSWAI	TSBCK	TFFCA	0	0	0	0
W								
RESET:	0	0	0	0	0	0	0	0

TEN — Timer Enable  
 1 = Allows the timer to function normally.  
 0 = Disables the main timer, including the counter.

**MC68HC812A4 registers**

**TMKS1**

	Bit 7	6	5	4	3	2	1	Bit 0
R	TOI	0	TPU	TDRB	TCRE	PR2	PR1	PR0
W								
RESET:	0	0	1	1	0	0	0	0

PR2, PR1, PR0 — Timer Prescaler Select  
 These three bits select the frequency of the timer prescaler clock derived from the Bus Clock

**9S12C32 registers**

**TSCR2**

	Bit 7	6	5	4	3	2	1	Bit 0
R	TOI	0	0	0	TCRE	PR2	PR1	PR0
W								
RESET:	0	0	0	0	0	0	0	0

PR2, PR1, PR0 — Timer Prescaler Select  
 These three bits select the frequency of the timer prescaler clock derived from the Bus Clock