Last Name: _____ First Name: _____

Jonathan W. Valvano March 2, 2005, 1:00pm-1:50pm

This is a closed book exam. No notes or calculators are allowed, just a pencil and eraser. You must put your answers in the answer boxes only, information written outside the box will not be graded. You have 50 minutes, so please allocate your time accordingly. ***Please read the entire quiz before starting.***

(5) Question 1. What is the value of an 8-bit unsigned binary fixed-point number (resolution is 2^{-3}, which equals 1/8) if the integer stored in memory is 25?

For questions 2-6, the definition is given and you are asked to give the correct term described by that definition. Since there are more terms than definitions, not all terms will be used. *Answer each as A through R.*

(4) Question 2. The situation when the presence of the debugger itself causes the software/hardware system to operate abnormally.

(4) Question 3. A type of logic that has only two output states, low or off.

(4) Question 4. A debugging technique that fixes all its inputs to specific values and can be repeated over and over.

(4) Question 5. A type of logic in which the output can be high, low, or off.

(4) Question 6. A system in which the time between when new input is ready and the time when the input is read by the software is small and bounded.

A) high speed CMOS	F) busy waiting	K) tristate	P) latency
B) Schottky	G) real-time	L) desk check	Q) invasiveness
C) atomic	H) nonvolatile	M) embedded	R) instrument
D) blind cycle	I) intrusive	N) friendly	
E) volatile	J) open collector	O) stabilize	

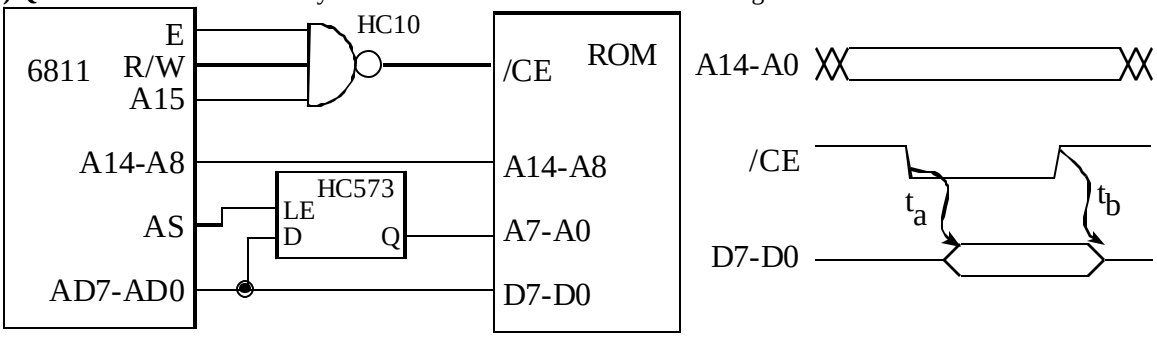
(5) Question 7. A signed fixed-point system has a range of values from -10.00 to 10.00 with a resolution of 10^{-2}. Note: 10^{-2} equals 0.01. With which of the following **data types** should the software variables be allocated? When more than one answer is possible choose the most space efficient type.

A) `unsigned char`	B) `char`	C) `float`	D) `unsigned long`
E) `unsigned short`	F) `short`	G) `double`	H) `long`

(20) Question 8. Design a minimal-cost positive-logic address decoder for **YourDevice** in the following system.

RAM	$6000-$6FFF	Show	1) design steps,
YourDevice	$7000-$7FFF		2) equation
ROM	$E000-$FFFF		3) circuit.

(25) Question 9. There is a 32k by 8 bit PROM interfaced to a 6811 running at 2 MHz as shown below



Assume t_a = 120 ns, and t_b = 20ns. Assume a 5ns gate delay through the 74LS10 and 74HC573. Determine RDA and RDR. Give your answer in numerical form, defining 0ns at the start of the cycle.

read data available interval, which should be given in the form of (number,number), such as (100,500)	**read data required interval**, which should be given in the form of (number,number), such as (100,500)

(25) Question 10. Write one function that receives a single ASCII character from the SCI with echo. You may assume the SCI device is already initialized. You will use busy-wait synchronization. The following sequence of events should occur in this order: 1) wait for new data to be received by the SCI device; 2) receive this new data; 3) wait for the transmit channel to be idle; 4) transmit this new data back (echo); 5) return by value this new data. I want you to directly access the SCI I/O device registers, rather than calling existing functions like **`SCI_InChar`** and **`SCI_OutChar`**. *Comments and programming style will be graded.*

(10) Part a) Show the code that will be placed in the **`SCI.h`** file

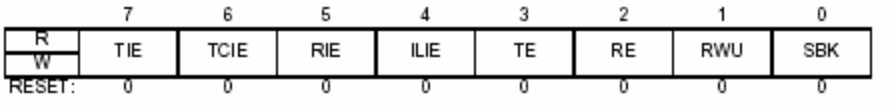
(15) Part b) Show the code that will be placed in the **`SCI.c`** file

	7	6	5	4	3	2	1	0
R	0	0	0	SBR12	SBR11	SBR10	SBR9	SBR8
W								
RESET:	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
R	SBR7	SBR6	SBR5	SBR4	SBR3	SBR2	SBR1	SBR0
W								
RESET:	0	0	0	0	0	1	0	0

Figure 3-2 SCI Baud Rate Registers (SCI BDH/L)

baud rate = SCI module clock / (16 x BR), where BR is the content of the SCI baud rate registers, bits SBR12 through SBR0.



	7	6	5	4	3	2	1	0
R	TIE	TCIE	RIE	ILIE	TE	RE	RWU	SBK
W								
RESET:	0	0	0	0	0	0	0	0

Figure 3-4 SCI Control Register 2 (SCICR2)

TE — Transmitter Enable Bit

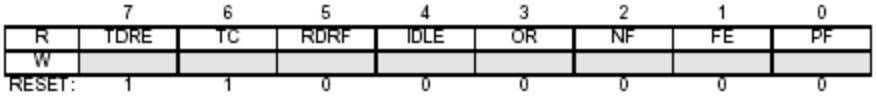
TE enables the SCI transmitter and configures the TXD pin as being controlled by the SCI. The TE bit can be used to queue an idle preamble.

1 = Transmitter enabled
0 = Transmitter disabled

RE — Receiver Enable Bit

RE enables the SCI receiver.

1 = Receiver enabled
0 = Receiver disabled



	7	6	5	4	3	2	1	0
R	TDRE	TC	RDRF	IDLE	OR	NF	FE	PF
W								
RESET:	1	1	0	0	0	0	0	0

Figure 3-5 SCI Status Register 1 (SCISR1)

TDRE — Transmit Data Register Empty Flag

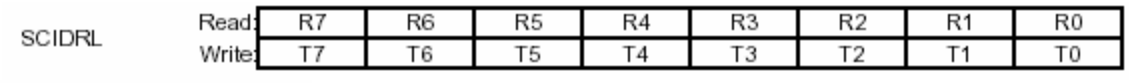
TDRE is set when the transmit shift register receives a byte from the SCI data register. When TDRE is 1, the transmit data register (SCIDRH/L) is empty and can receive a new value to transmit.Clear TDRE by reading SCI status register 1 (SCISR1), with TDRE set and then writing to SCI data register low (SCIDRL).

1 = Byte transferred to transmit shift register; transmit data register empty
0 = No byte transferred to transmit shift register

RDRF — Receive Data Register Full Flag

RDRF is set when the data in the receive shift register transfers to the SCI data register. Clear RDRF by reading SCI status register 1 (SCISR1) with RDRF set and then reading SCI data register low (SCIDRL).

1 = Received data available in SCI data register
0 = Data not available in SCI data register



SCIDRL	Read:	R7	R6	R5	R4	R3	R2	R1	R0
	Write:	T7	T6	T5	T4	T3	T2	T1	T0

Figure 3-7 SCI Data Registers

TCNT

	Bit 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	Bit 0
R W	tcnt 15	tcnt 14	tcnt 13	tcnt 12	tcnt 11	tcnt 10	tcnt 9	tcnt 8	tcnt 7	tcnt 6	tcnt 5	tcnt 4	tcnt 3	tcnt 2	tcnt 1	tcnt t 0
RESET:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The 16-bit main timer is an up counter.

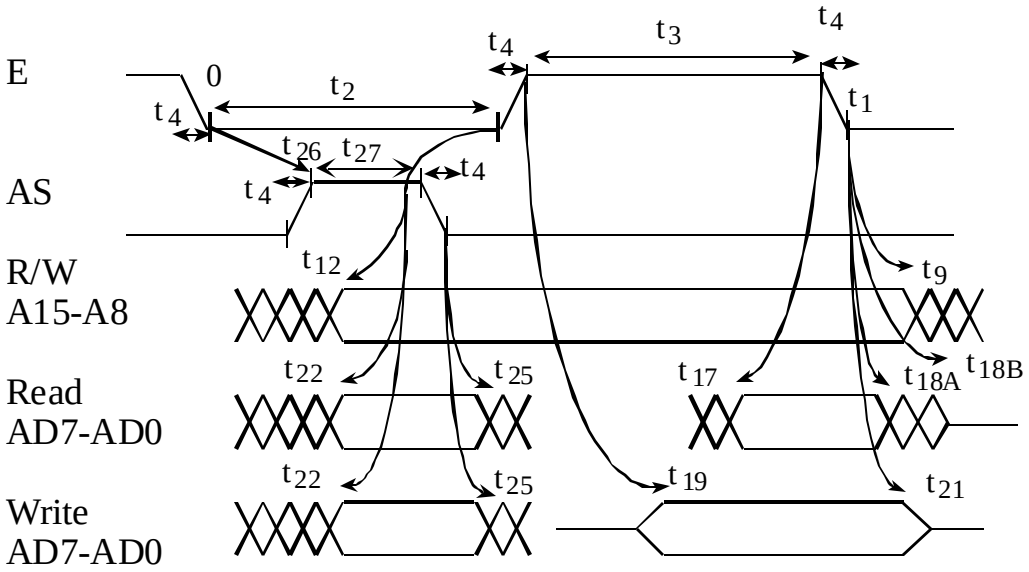
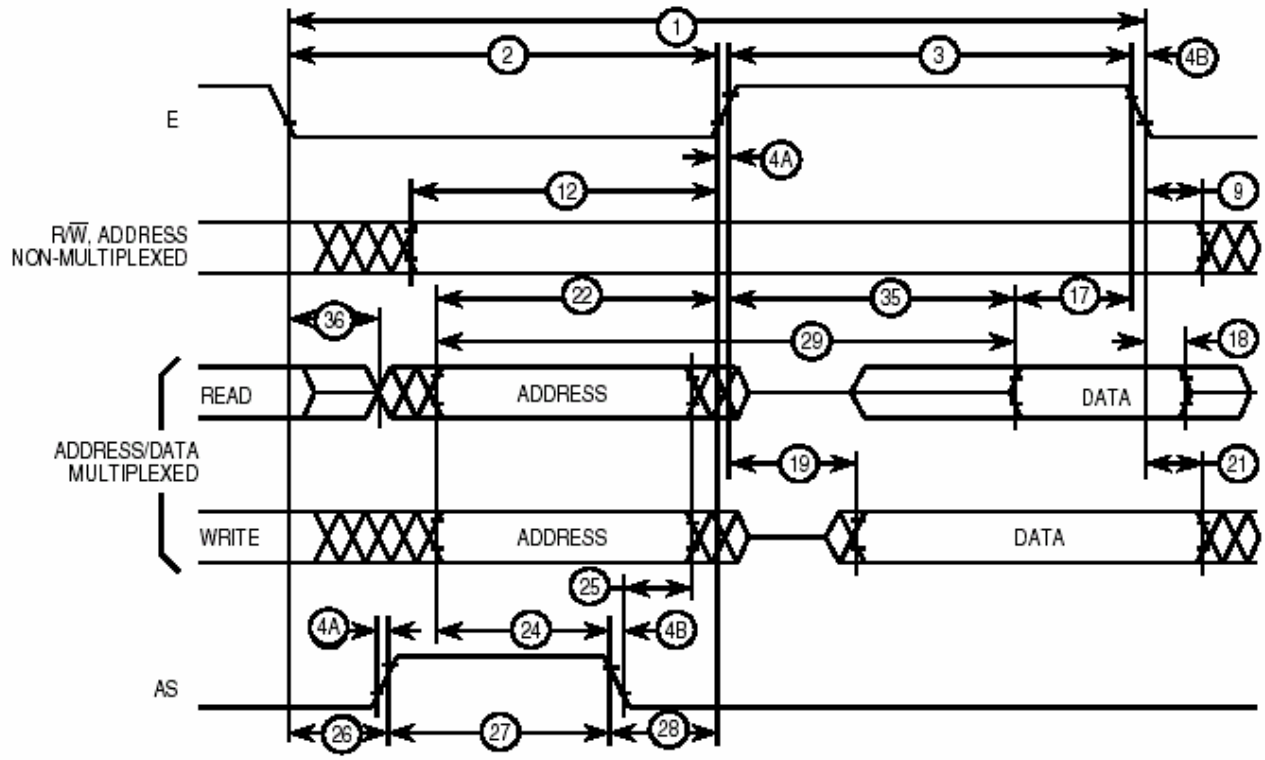


Figure 9.34. Simplified bus timing for the 6811 in expanded mode.

Num	Characteristic	1.0 MHz	**2.0 MHz**	2.1 MHz	Units
	Frequency	1.0	**2.0**	2.1	MHz
t_1	Cycle Time	1000	**500**	476	ns
t_2	Pulse Width E low	480	**230**	218	ns
t_3	Pulse Width E high	480	**230**	218	ns
t_4	rise/fall time	20	**20**	20	ns
t_9	address hold time	95.5 min	**33 min**	30 min	ns
t_{12}	A15-A8,R/W valid time	281.5 min	**94 min**	85 min	ns
t_{17}	Read data setup time	30 min	**30 min**	30 min	ns
t_{18A}	Read data hold time	10 min	**10 min**	10 min	ns
t_{18B}	Read data goes hiZ	145.5 max	**83 max**	80 max	ns
t_{19}	Write data delay time	190.5 max	**128 max**	125 max	ns
t_{21}	Write data hold time	95.5 min	**33 min**	30 min	ns
t_{22}	A7-A0 valid time	271.5 min	**84 min**	75 min	ns
t_{25}	A7-A0 hold time	95.5 min	**33 min**	30 min	ns
t_{26}	E to AS rise time	115.5	**53**	50	ns
t_{27}	AS pulse width	221	**96**	90	ns



Note: Measurement points shown are 20% and 70% of V_{DD}.

Figure 10-14. Multiplexed Expansion Bus Timing Diagram