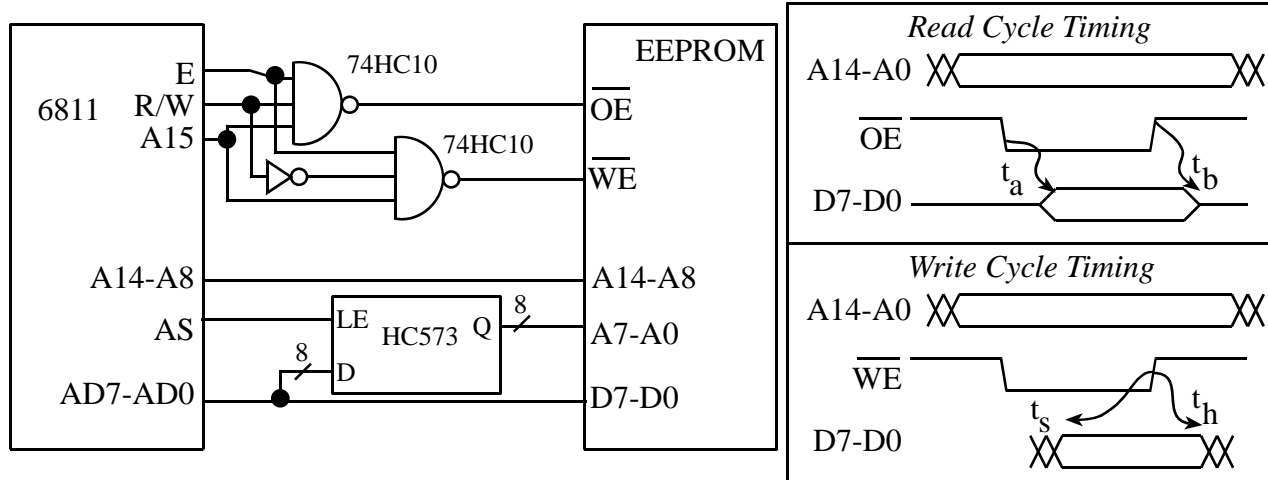


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First: _____ Last: _____

November 16, 2007, 1:00pm-1:50pm. This is an open book test No electronic devices allowed. You have 50 minutes, so please allocate your time accordingly. **Please read the entire quiz before starting.**

(15) Question 1. This interface connects a 32k by 8-bit EEPROM to a 6811 running at **1 MHz**. Assume the gate delay through each 74HC10 digital logic gate is [5ns min, 15ns max]. The full address decoder selects addresses \$8000 to \$FFFF. The EEPROM has two control signals, \overline{OE} and \overline{WE} . During a read cycle $\overline{WE}=1$ and $\overline{OE}=0$, and during a write cycle, $\overline{WE}=0$ and $\overline{OE}=1$. t_a and t_b are the EEPROM read cycle timing parameters. t_s and t_h are the EEPROM write cycle timing parameters.



What is the largest value possible for t_a so that read data available overlaps read data required?

(25) Question 2. The goal of this interface is to provide 8 digital inputs using a 74HC165 and the SPI port. Since the 74HC165 can run at 56 MHz, you can initialize the 9S12 SPI to its maximum frequency. The chip enable, CE/, will be grounded to activate the parallel-in serial-out shift register. The serial input, D_s, will be grounded. Eight external digital inputs will be connected to D₀ through D₇. The parallel load, PL, signal will be connected to a regular 9S12 output, PM3. The serial data out, Q7, of the 74HC165 will be interfaced to the 9S12 MISO SPI, PM2. The serial clock input, CP, of the 74HC165 will be interfaced to the 9S12 Sclk output, PM5. First, the software will load the digital inputs into the 74HC165 by making PL=0, making PL=1. Next, the software will initiate the SPI causing 8-bits to transfer from the 74HC165 to the 9S12. A rising edge on CP causes a shift output.

Part a) Show the ritual that initializes the interface. Be friendly. In particular, finish these C lines

```
void SPI_Init(void){
```

```
    DDRM
```

```
    PTM
```

```
    SPICR1
```

```
    SPICR2
```

```
    SPIBR =
```

```
}
```

Part b) Write a C function that reads the 8-bit digital input, returning the result

```
unsigned char SPI_In(void){
```

(10) Question 3. Design a minimal-cost negative-logic address decoder for *YourDevice* in the following system. The inputs are A15, A14, ...A0 and the output is **Select**. Negative logic means **Select**=0 when *YourDevice* should be activated, and **Select**=1 when *YourDevice* is deactivated.

RAM	\$0000-\$0FFF	Show	1) design steps,
<i>YourDevice</i>	\$4000-\$400F		2) logic equation,
I/O	\$4010-\$401F		3) digital logic circuit.
ROM	\$C000-\$FFFF		

Give chip numbers, but not pin numbers (design just the decoder for *YourDevice*, not all of them)

(30) Question 4. Assume there is a noisy analog signal connected to PAD3. To improve signal to noise ratio, channel 3 will be sampled 4 times and the four digital outputs will be averaged. The ADC will be used in 10-bit, right-justified, unsigned format. Use output compare 7 to create a sampling rate of 1000 Hz. Assume the PLL is not running, so the E period is 250ns.

Part a) To what value should you initialize **ATDCTL2**? Give your answer in hex.

ATDCTL2 =

Part b) The goal is to initialize the ADC so that one start command will sample PAD3 exactly four times, no more no less. To what value should you initialize **ATDCTL3**? Give your answer in hex.

ATDCTL3 =

Part c) In order to reduce noise, the 10-bit ADC will be operated at the slowest possible rate. To what value should you initialize **ATDCTL4** so the ADC operates at 500 kHz? Choose the largest sample time (s=18). Give your answer in hex.

ATDCTL4 =

Part d) Show the output compare 7 ritual. The main program calls this OC7 ritual, the ADC initialization (as defined in Parts a, b, and c) and executes other unrelated tasks.

Part e) Show the entire output compare 7 interrupt service routine that implements the 1 kHz sampling. OC7 is interrupt number 15. In particular, every 1 ms, PAD3 is sampled four times and the global variable **Average** is updated with the average of the four samples. In order to start the four ADC conversions on PAD3, consider carefully what value should be written into **ATDCTL5**. After the four ADC conversions are finished, consider carefully which I/O registers contain the four 10-bit results of the ADC conversions of channel PAD3? I.e., choose from **ATDDR0**, **ATDDR1**, ... or **ATDDR7**. Assume **Average** is a global variable. Show all software executed in the ISR.

(20) Question 5. Design a circuit with three analog inputs V_0 , V_1 , V_2 and one analog output V_{out} . To get full credit, use exactly one op amp. Also, please use resistors larger than $10\text{ k}\Omega$, but less than $500\text{ k}\Omega$. Implement the following transfer function (show your work).

$$V_{\text{out}} = (1/2) * V_0 + (1/4) * V_1 + (1/8) * V_2$$

(Note: these gains are all positive and all less than one. E.g., 1/8 is one eighth not eight)