Jonathan W. Valvano First:_____ Last:_____
November 21, 2008, 2:00pm-2:50pm. Open book, open notes, calculator (no laptops, phones, devices with screens larger than a TI-89 calculator, devices with wireless communication). You have 50 minutes, so please allocate your time accordingly. ***Please read the entire quiz before starting***.

(20) Question 1. Design and implement a software function that performs logarithm base 10. The input of the function is an unsigned 16-bit fixed-point number with a resolution of 0.01, and the output is a signed decimal fixed-point number with a resolution of 0.01. For example $\log_{10}(0.01)$=-2.00, $\log_{10}(0.10)$=-1.00, $\log_{10}(1.00)$=0.00, $\log_{10}(2.54)$=0.41, $\log_{10}(10.00)$=1.00, $\log_{10}(20.00)$=1.30, $\log_{10}(100.00)$=2.00. No floating is allowed.

```
// input: data is integer part of the fixed-point number Δ=0.01
// output: integer part of the fixed-point number Δ=0.01
short log10(unsigned short data){
```

(20) Question 2. You are given two digital lines on PT7 and PT6 and are asked to implement an SPI output channel with PT7 as its clock and PT6 as its data. The mode will mimic CPOL=0, CPHA=0.
Part a) Show the ritual that initializes the interface. Be friendly. Show comments.

```
void SPI2_Init(void){
```

Part b) Write a C function that outputs one 8-bit digital value to this SPI channel. Make it run as fast as possible. Be friendly. Show comments.

```
void SPI2_Out(unsigned char data){
```

(30) Question 3. Consider the 6811/EEPROM system designed in Lab 8. The system will be redesigned to provide for more output pins. Rather than connecting a 74HC595 to SPI, using 4 pins to create 8 outputs, we will connect a 74HC374 octal D flip-flip directly to the address/data bus of the 6811. You need to redesign the Lab 8 computer to connect both an external EEPROM and an external 74HC374 to the address data bus of the 6811. This 8-bit output port will be placed at $4000, and respond only to write cycles. In particular, when the software writes to $4000, new 8-bit data will be available on the outputs of the 74HC374. Read cycles to $4000 have no effect. The following is the memory map of the augmented Lab 8 system

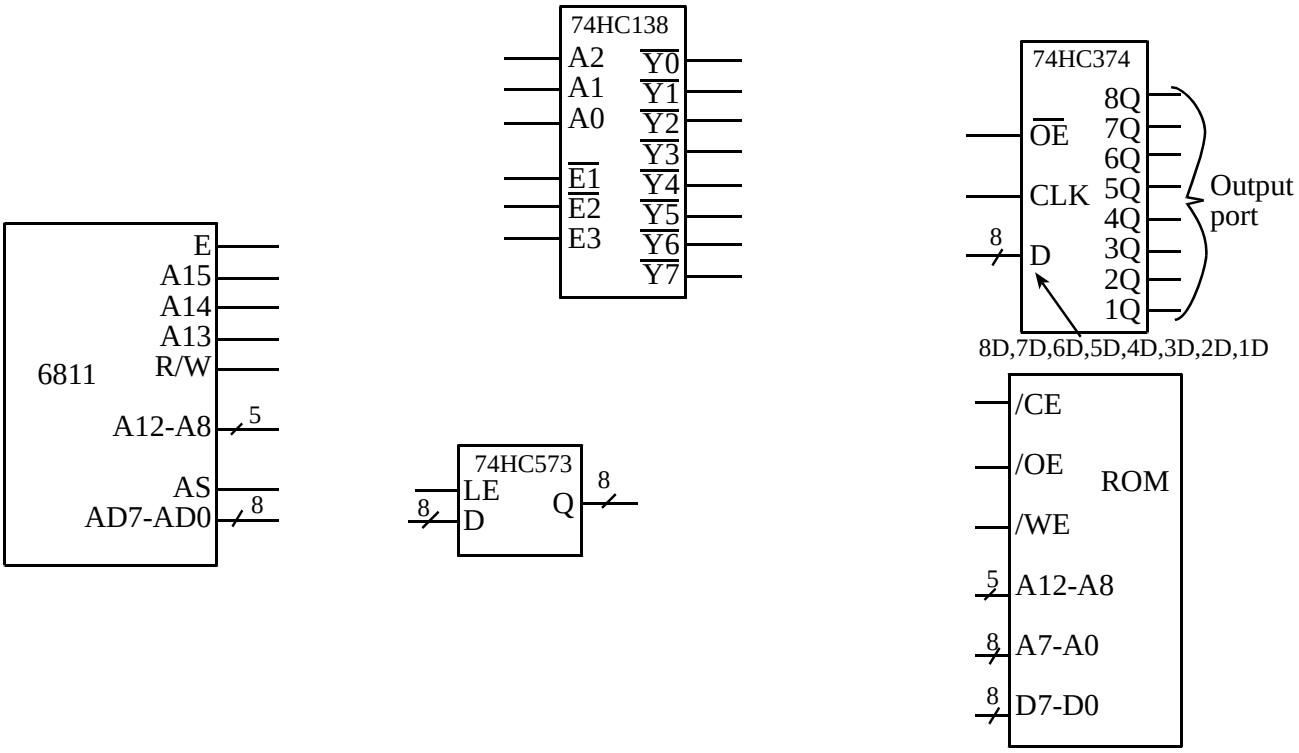
$0000 to $01FF 512 bytes of internal RAM (globals and stack)
$1000 to $103F input/output ports
$4000 the new 8-bit output port using a 74HC374
$B600 to $B7FF 512 bytes of EEPROM (your program)
$BF00 to $BFFF internal boot loader (to download programs)
$E000 to $FFFF your external 8K EEPROM

Part a) Show the design of the address decoder for **BOTH** the 74HC374 and the EEPROM

Part b) Show the design steps to create the 74HC374 control signals. Fill in this table

Select	R/W	E	CLK	/OE	action
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0			
1	1	1			

Part c) Interface both the EEPROM and the 74HC374 to the 6811. Additional gates are allowed, but not needed.

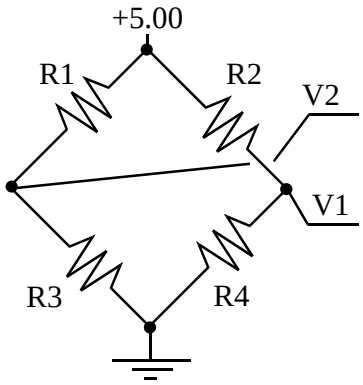


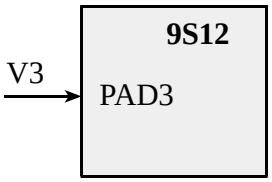
Part d) Assuming the E clock period is 2 MHz and the delay through the 74HC138 is 10ns, what are WDA and WDR for this 6811/74HC374 interface.

(30) Question 4. You will design the analog hardware for a data acquisition system to measure displacement (vibrations, distance). The range of displacement is -1 to +1 mm. Each resistance in the bridge is linear to displacement having a sensitivity of 10 Ω/mm. At zero displacement all four resistors are 1000 Ω. The displacement signal exists in the 0 to 1000 Hz frequency band.
Part a) Fill in the following design table. The bridge output (V2-V1) is a differential voltage.

Displacement (mm)	R1 (Ω)	R2 (Ω)	R3 (Ω)	R4 (Ω)	V2 (V)	V1 (V)	V2-V1 (V)	V3 (V)	ADC result
-1	1010	990	990	1010					
0	1000	1000	1000	1000					
1	990	1010	1010	990					

Part b) A good CMRR is required. Design the analog circuit using just the single +5V supply mapping the bridge output (V2-V1) into the ADC input channel 3 (V3). You do not need to add an antialiasing analog low pass filter. Show chip numbers, resistor values, but not pin numbers.



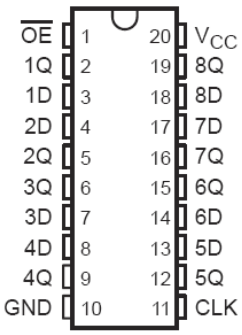


SN54HC374, SN74HC374
OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

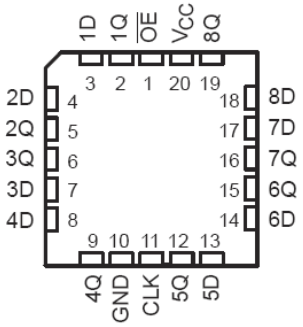
SCLS141E – DECEMBER 1982 – REVISED AUGUST 2003

- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State True Outputs Can Drive Up To 15 LSTTL Loads
- Eight D-Type Flip-Flops in a Single Package
- Full Parallel Access for Loading
- Low Power Consumption, 80-μA Max I_{CC}
- Typical t_{pd} = 14 ns
- ±6-mA Output Drive at 5 V
- Low Input Current of 1 μA Max

SN54HC374 . . . J OR W PACKAGE
SN74HC374 . . . DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54HC374 . . . FK PACKAGE
(TOP VIEW)



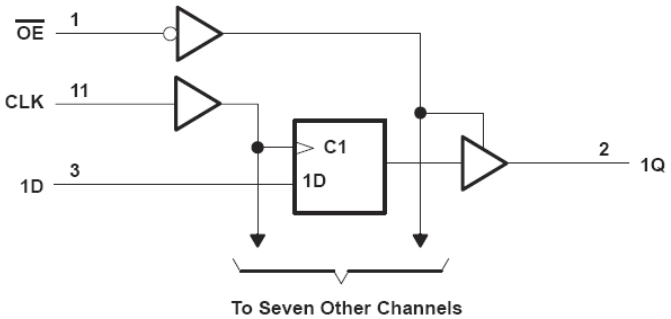
$\overline{OE}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
$\overline{OE}$	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_0
H	X	X	Z

logic diagram (positive logic)



You may assume the setup time is 30ns and the hold time is 5ns relative to the rising edge of CLK.

3-to-8 line decoder/demultiplexer; inverting 74HC/HCT138

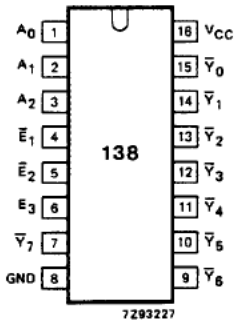


Fig.1 Pin configuration.

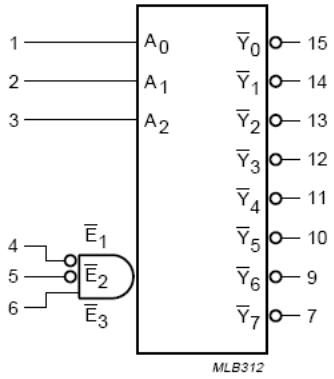


Fig.2 Logic symbol.

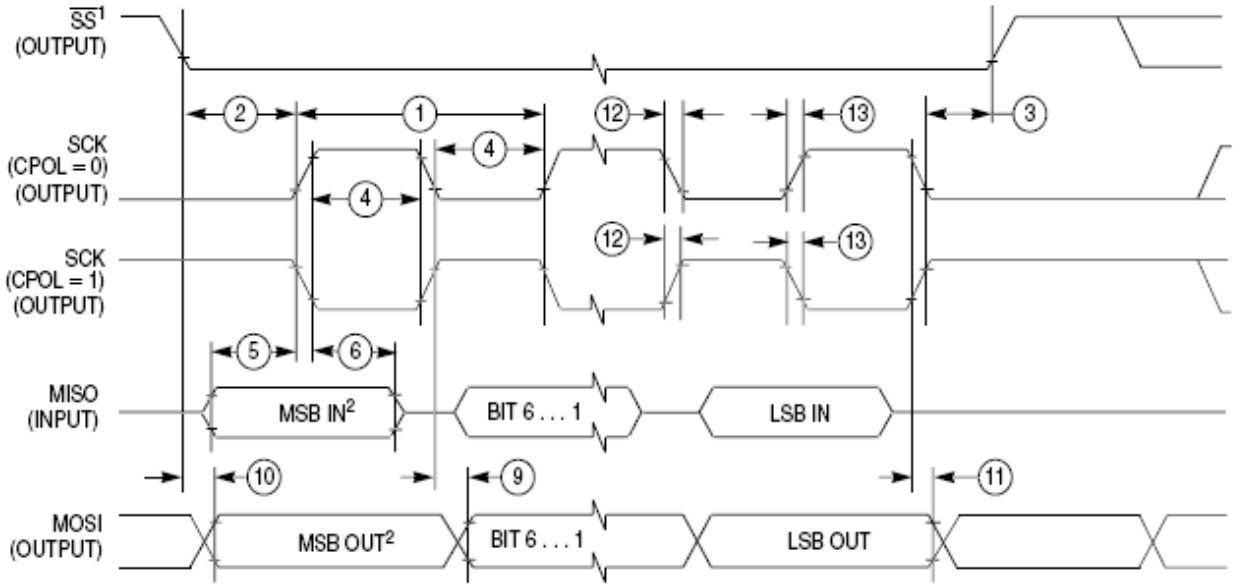
3-to-8 line decoder/demultiplexer; inverting 74HC/HCT138

FUNCTION TABLE

INPUTS						OUTPUTS							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{Y}_0$	$\overline{Y}_1$	$\overline{Y}_2$	$\overline{Y}_3$	$\overline{Y}_4$	$\overline{Y}_5$	$\overline{Y}_6$	$\overline{Y}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

Notes

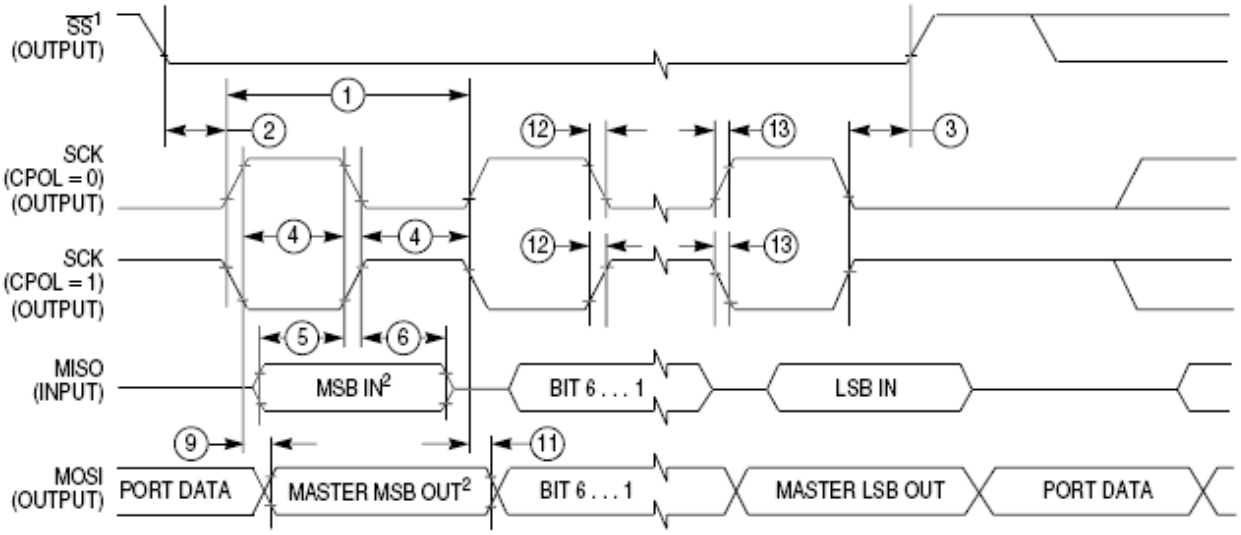
1. H = HIGH voltage level
   L = LOW voltage level
   X = don't care



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure A-6. SPI Master Timing (CPHA=0)

In Figure A-7 the timing diagram for master mode with transmission format CPHA=1 is depicted.



1. If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure A-7. SPI Master Timing (CPHA=1)