Jonathan W. Valvano First:_____ Last:_____

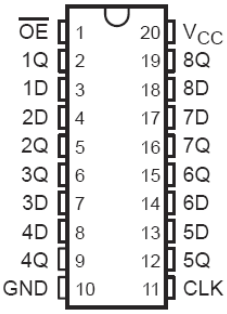
November 20, 2009, 2:00pm-2:50pm. Open book, open notes, calculator (no laptops, phones, devices with screens larger than a TI-89 calculator, devices with wireless communication). You have 50 minutes, so please allocate your time accordingly. ***Please read the entire quiz before starting***.

**SN54HC374, SN74HC374**
**OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOPS**
**WITH 3-STATE OUTPUTS**

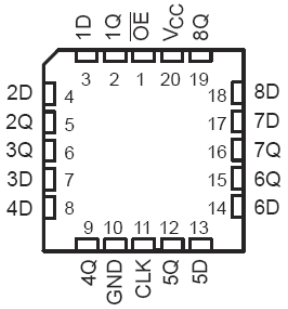
SCLS141E – DECEMBER 1982 – REVISED AUGUST 2003

- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State True Outputs Can Drive Up To 15 LSTTL Loads
- Eight D-Type Flip-Flops in a Single Package
- Full Parallel Access for Loading
- Low Power Consumption, 80-μA Max $I_{CC}$
- Typical $t_{pd}$ = 14 ns
- ±6-mA Output Drive at 5 V
- Low Input Current of 1 μA Max

SN54HC374 . . . J OR W PACKAGE
SN74HC374 . . . DB, DW, N, NS, OR PW PACKAGE
(TOP VIEW)




SN54HC374 . . . FK PACKAGE
(TOP VIEW)



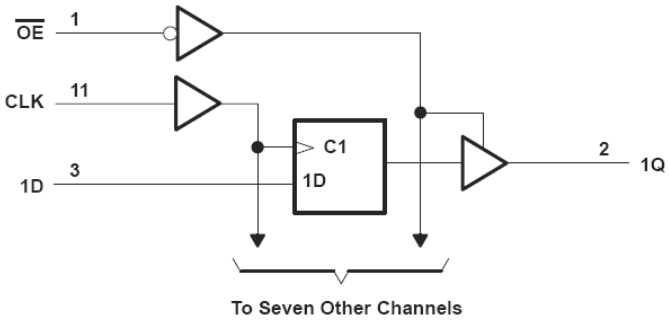

$\overline{OE}$ does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

FUNCTION TABLE
(each flip-flop)

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | CLK | D | Q |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | $Q_0$ |
| H | X | X | Z |

**logic diagram (positive logic)**




You may assume the setup time is 30ns and the hold time is 5ns relative to the rising edge of CLK.

**(15) Question 1.** The inputs to a software function **x**, **y** are both unsigned **n**-bit integers. You may assume **n** is an even number greater than 8. I.e., **n** is an element of the set {8, 10, 12, 14, 16, …}
(5) Part a) How many bits is the integer product **x***y**? Put your answer in the box.

(5) Part b) How many bits is the integer quotient **x**/**y** (assuming **y** is not zero)? Put your answer in the box.

(5) Part c) How many bits is the integer square root of **x**? For example the sqrt(5) is 2. Put your answer in the box.

If you can not solve this problem for the general case n, for partial credit solve it for **n**=8.

**(5) Question 2.** There were five $V_{DD}$ pins on the MC9S12C128: $V_{DD1}$ $V_{DD2}$ $V_{DDA}$ $V_{DDR1}$ and $V_{DDX}$. Why did we place a separate 0.1 μF ceramic capacitor physically close each of these five pins on the MC9S12C128 layout? All choices are true statements; pick the one that best answers the question?

**A)** The regulator needs capacitance at its output in order to stabilize the +5V supply. The manufacturer of each regulator will suggest appropriate capacitance values and capacitor types at its input and output.

**B)** A pi filter (CLC) can be used to separate digital noise from analog circuits. It works by preventing high frequency current spikes on the digital circuits from causing voltage spikes on the analog circuits. Similar filters can be made with ferrite bead cores.

**C)** CMOS logic needs charge whenever a digital line rises or falls. Current through the resistance of the wire will cause a voltage drop. The closer the capacitor is to the chip, the less voltage drop there will be on the $V_{DD}$ pin.

**D)** Capacitors are extremely important for the phase lock loop (PLL). In particular, the proper choice of capacitors is required for the PLL to lock. In fact, one usually knows in advance what frequency the PLL will be used at (e.g., 24 MHz) and tunes the capacitors for that frequency.

**E)** Capacitors are extremely important for the crystal oscillator (EXTAL and XTAL). In particular, the proper choice of capacitors is required for the E clock to oscillate. The position of the capacitors in your layout is critical for the clock to operate.

**F)** Capacitors are an important part of a low pass filter. For a single pole low pass filter made with a resistor and capacitor, we can estimate the time constant as R*C; the frequency response of such a system is about $1/(2\pi RC)$.

Put your answer in the box.

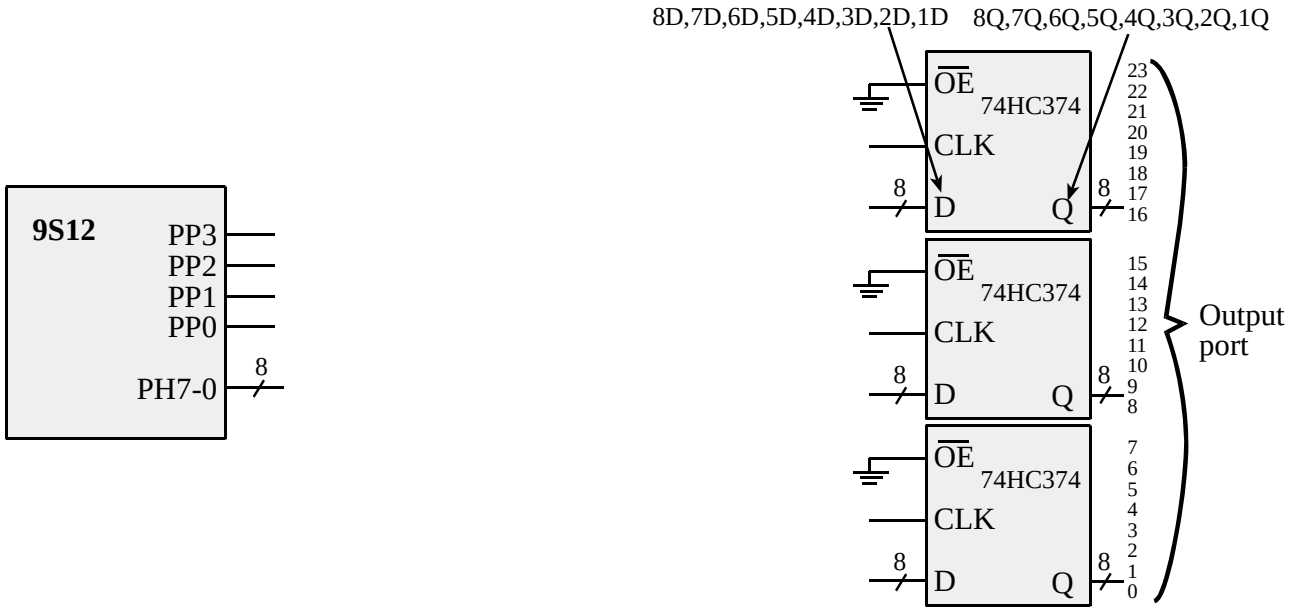
**(20) Question 3.** Write a C program that scans a buffer and returns the **mode** of the data. Mode is the value that occurs most frequently. For example, the mode of {1,**2**,3,4,5,**2**,3,6,3,8,**2**,8,0,**2**} is 2 because 2 occurs fours times and the other values occur less than four. If there is more than one mode, you can return any one of them. You are passed a pointer a 1000-point data buffer of 8-bit binary fixed point voltages with a range of values of -2 to +1.984375V. This range of values is -128/64 to +127/64 volts. The resolution is 1/64 volts. The size of the buffer is always 1000 elements. Hint allocate an array and count the number of occurrences for each possible value. The prototype is

```
char FindMode(char *pt);
```

A typical calling sequence is

```
char Buffer[1000];  // units are 1/64 volts
char Mode;
void main(void){
    // the main program fills up Buffer with 1000 data values
  Mode = FindMode(Buffer); // your program scans Buffer, returns mode
```

**(35) Question 4.** You are given 12 9S12 pins to work with, but need 24 digital output lines. There are two approaches to making more outputs: serial and parallel. This question uses the parallel method.
(10) Part a) Show the hardware interface between the 9S12 and the three 74HC374 octal D flip flops.

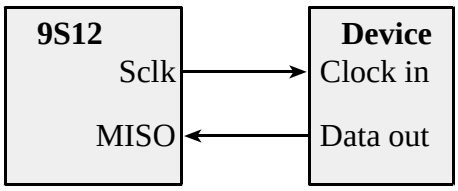


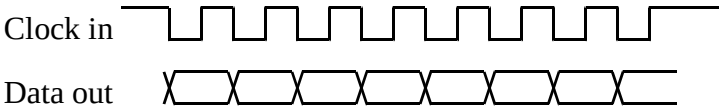

(10) Part b) Write an initialization ritual. You will need to use private permanently-allocated variables. Initially clear all output port bits to zero.

(15) Part c) Write a C function that sets individual bits in the interface. The bits are numbered from 23 to 0 from top to bottom. Calling your **`SetPort(23)`** will set the output pin in bit 7 of the top most 74HC374. The input parameter of this function is a number from 0 to 23.

(0) Part d) Write a C function that clears individual bits in the interface. The bits are numbered from 23 to 0 from top to bottom. Calling your **`ClrPort(8)`** will clear the output pin in bit 0 of the middle 74HC374. The input parameter of this function is a number from 0 to 23.

**(10) Question 5.** There is an 8-bit input-only device interfaced to SPI. The device timing is shown. During the idle condition, the clock should be high. The device shifts data out on the falling edge.




To what mode should SPI be initialized?

**A)** CPOL = 0; CPHA = 0
**B)** CPOL = 1; CPHA = 0
**C)** CPOL = 0; CPHA = 1
**D)** CPOL = 1; CPHA = 1

Put your answer in the box.

**(15) Question 6.** Design an analog circuit with the following transfer function $V_{out} = 5\text{-}2*V_{in}$. The input is a single voltage (not differential). The input range is 0 to 2.5V and the output range is 0 to 5V. Use an analog reference and one rail to rail op amp. Show your work and label all chip numbers and resistor values. You do not have to show pin numbers.