Jonathan W. Valvano First:__________________ Last:_______________________

April 18, 1:00pm-1:50pm. Open book, open notes, calculator (no laptops, phones, devices with screens larger than a TI-89 calculator, devices with wireless communication). Please don't turn in any extra sheets. You have 50 minutes, so please allocate your time accordingly. ***Please read the entire quiz before starting***.

**(20) Question 1.** Review the attached data sheets for the 9S12DP512. It uses a multiplexed address/data bus for its A15-A0/D15-D0 like the 6811 uses for its A7-A0/D7-D0. You may assume the E clock is 25 MHz. making the period 40 ns. The rise and fall times of the E clock are 1 ns. Just like the 6811 timing, we define time 0 at the start of the cycle, shown as the first dotted line in the figure. The second dotted line occurs at half way through the cycle, time = 20ns, and the third line is at 40ns.

**(10) Part a)** Determine the **read data available** interval. Show your work and give the interval in actual numbers in ns.

**(10) Part b)** Determine the **write data required** interval. Show your work and give the interval in actual numbers in ns.

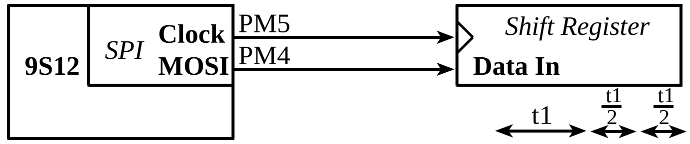
**(10) Question 2.** Design a **fully-decoded** positive-logic address decoder for *YourDevice* in the following system. The inputs are A15, A14, …A0 and the output is **Select**. Positive logic means **Select**=1 when *YourDevice* should be activated, and **Select**=0 when *YourDevice* is deactivated.

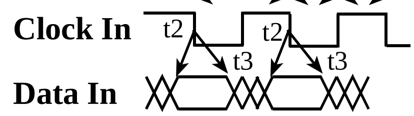
| | |
|---|---|
| RAM | \$0000-\$0FFF |
| *YourDevice* | \$4000-\$5FFF |
| I/O | \$8010-\$801F |
| ROM | \$C000-\$FFFF |

Show 1) design steps,
2) logic equation,
3) digital logic circuit.

Give chip numbers, but not pin numbers (design just the decoder for *YourDevice*, not all of them)

**(25) Question 3.** The data and clock outputs of the SPI are connected to the inputs of a shift register. Assume the SPI clock has a 50% duty cycle. The period of the SPI clock is $\mathbf{t_1}$. The data should be shifted out of the SPI on the rising edge of **Clock**, because it is clocked into the shift register on the falling edge. The time $\mathbf{t_2}$ = 200ns is the time before the rising edge of **Clock** that the data must be valid. The time $\mathbf{t_3}$ = 50ns is the time after that same rising edge of **Clock** that the data must continue to be valid. The SPI data sheet is attached.




Part a) What is the smallest $\mathbf{t_1}$ clock period that reliably transverses data from one shift register to the other?

Part b) What are the correct values for CPOL and CPHA?

```
CPOL =
CPHA =
```

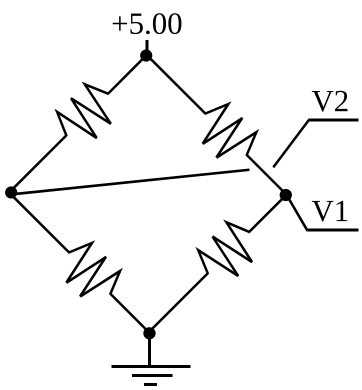
Part c) Write a C function that writes an 8-bit digital number to the shift register. Assume the SPI is already initialized.

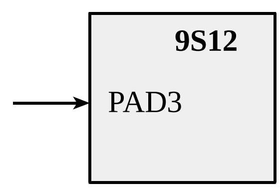
```
void SPI_Out(unsigned char data){
```

**(45) Question 4.** You will design a data acquisition system to measure force. The range of force is -10 to 10 N. The force signal exists in the 0 to 99 Hz frequency band. You will measure the ADC at a fixed rate, convert each sample to signed decimal fixed-point, and write each fixed-point measurement into global variable called **`Force`** (which is the integer part of the fixed-point number). The ADC sampling must occur in real-time using an output compare periodic interrupt **channel 5**.

Part a) Choose the sampling rate. Explain why you chose that value.

Part b) The sensitivity of the bridge output is 0.025 V/N, meaning the differential voltage (V2-V1) varies from -0.25 to +0.25 volts. However, both V1 and V2 are around 2.5V (more specifically V2 varies from 2.375 to 2.625 V, while V1 varies from 2.625 to 2.375 volts). A good CMRR is required. Design the analog circuit mapping the bridge output into the ADC input channel 3. (You do not have to add an antialiasing analog low pass filter.) Show chip numbers, resistor values, but not pin numbers.




Part c) Assuming the only error occurs in the 10-bit ADC, what is the expected force measurement resolution in Newtons (N)?

Part d) Write the **entire program** that implements this real time data acquisition system. You are allowed to call the following functions (without showing the implementations of these functions).

```
PLL_Init();        // initializes the PLL, E clock to 24 MHz
ADC_Init();        // initializes the ADC
data=ADC_In(0x83); // returns 10-bit sample from chan 3, 0 to 1023
```

If you need other functions, you will have to show their implementations. Be sure to include the software that maps unsigned ADC (0 to 1023) into signed fixed-point (resolution you choose in part c). Include the output compare 5 initialization and ISR.

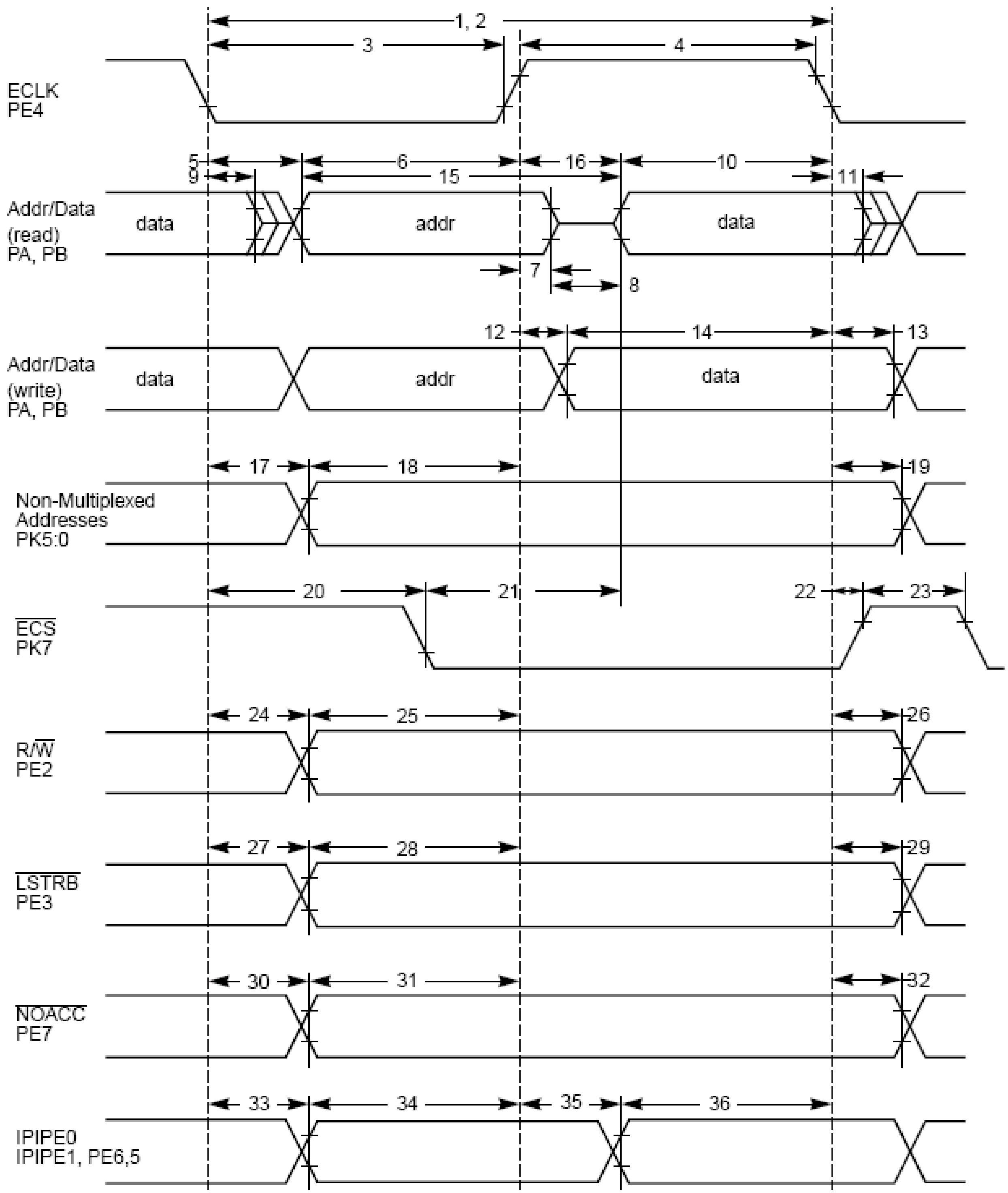
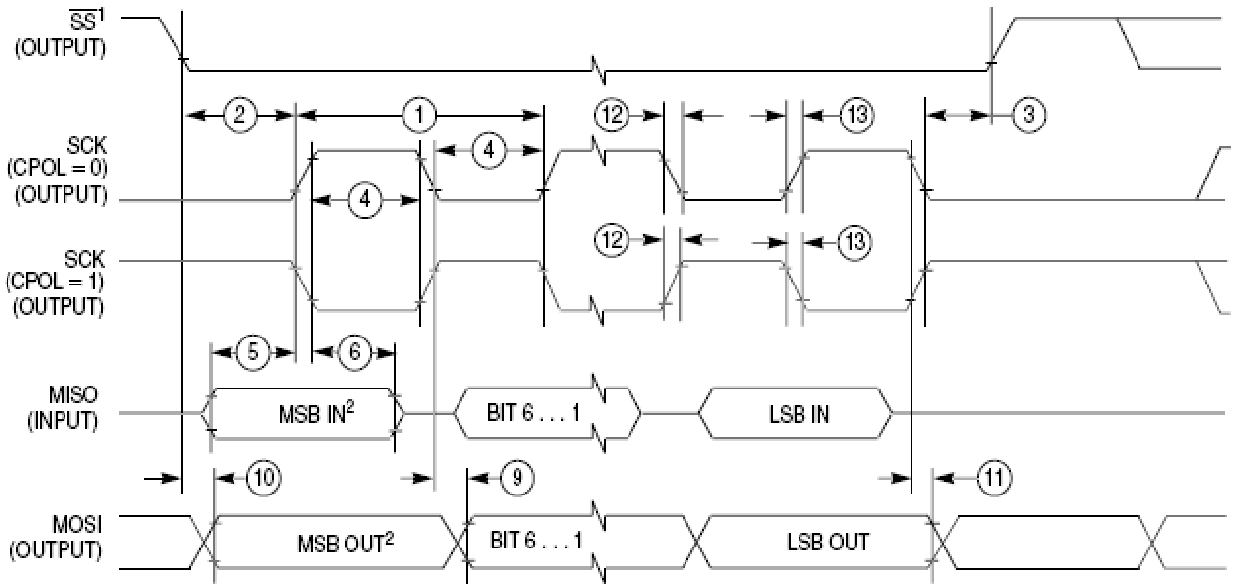



**Figure A-10 General External Bus Timing**

**Table A-21 Expanded Bus Timing Characteristics**

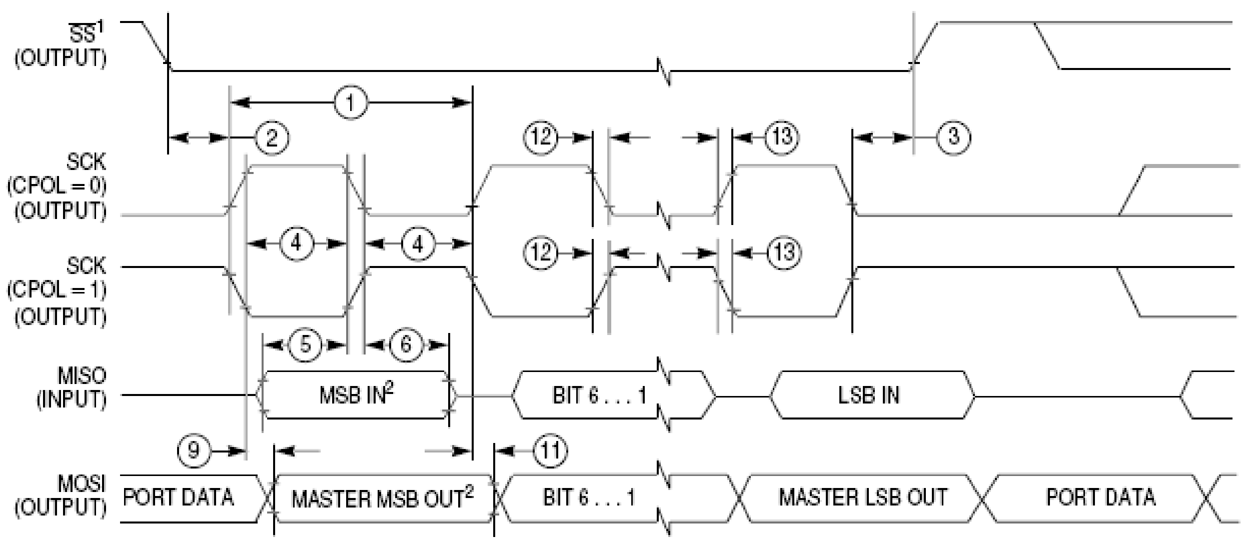
| Conditions are shown in **Table A-4** unless otherwise noted, $C_{LOAD}$ = 50pF | | | | | | | |
|---|---|---|---|---|---|---|---|
| **Num** | **C** | **Rating** | **Symbol** | **Min** | **Typ** | **Max** | **Unit** |
| 1 | P | Frequency of operation (E-clock) | $f_o$ | 0 | - | 25.0 | MHz |
| 2 | P | Cycle time | $t_{cyc}$ | 40 | - | - | ns |
| 3 | D | Pulse width, E low | $PW_{EL}$ | 19 | - | - | ns |
| 4 | D | Pulse width, E high[1] | $PW_{EH}$ | 19 | - | - | ns |
| 5 | D | Address delay time | $t_{AD}$ | - | - | 8 | ns |
| 6 | D | Address valid time to E rise ($PW_{EL}-t_{AD}$) | $t_{AV}$ | 11 | - | - | ns |
| 7 | D | Muxed address hold time | $t_{MAH}$ | 2 | - | - | ns |
| 8 | D | Address hold to data valid | $t_{AHDS}$ | 7 | - | - | ns |
| 9 | D | Data hold to address | $t_{DHA}$ | 2 | - | - | ns |
| 10 | D | Read data setup time | $t_{DSR}$ | 13 | - | - | ns |
| 11 | D | Read data hold time | $t_{DHR}$ | 0 | - | - | ns |
| 12 | D | Write data delay time | $t_{DDW}$ | - | - | 7 | ns |
| 13 | D | Write data hold time | $t_{DHW}$ | 2 | - | - | ns |
| 14 | D | Write data setup time[(1)] ($PW_{EH}-t_{DDW}$) | $t_{DSW}$ | 12 | - | - | ns |
| 15 | D | Address access time[(1)] ($t_{cyc}-t_{AD}-t_{DSR}$) | $t_{ACCA}$ | 19 | - | - | ns |
| 16 | D | E high access time[(1)] ($PW_{EH}-t_{DSR}$) | $t_{ACCE}$ | 6 | - | - | ns |
| 17 | D | Non-multiplexed address delay time | $t_{NAD}$ | - | - | 6 | ns |
| 18 | D | Non-muxed address valid to E rise ($PW_{EL}-t_{NAD}$) | $t_{NAV}$ | 13 | - | - | ns |
| 19 | D | Non-multiplexed address hold time | $t_{NAH}$ | 2 | - | - | ns |
| 20 | D | Chip select delay time | $t_{CSD}$ | - | - | 16 | ns |
| 21 | D | Chip select access time[(1)] ($t_{cyc}-t_{CSD}-t_{DSR}$) | $t_{ACCS}$ | 11 | - | - | ns |
| 22 | D | Chip select hold time | $t_{CSH}$ | 2 | - | - | ns |
| 23 | D | Chip select negated time | $t_{CSN}$ | 8 | - | - | ns |
| 24 | D | Read/write delay time | $t_{RWD}$ | - | - | 7 | ns |
| 25 | D | Read/write valid time to E rise ($PW_{EL}-t_{RWD}$) | $t_{RWV}$ | 14 | - | - | ns |
| 26 | D | Read/write hold time | $t_{RWH}$ | 2 | - | - | ns |




1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure A-6. SPI Master Timing (CPHA=0)**

In Figure A-7 the timing diagram for master mode with transmission format CPHA=1 is depicted.




1. If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

**Figure A-7. SPI Master Timing (CPHA=1)**

**Table A-21. SPI Master Mode Timing Characteristics**

| Num | C | Characteristic | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| 1 | P | SCK Frequency | $f_{sck}$ | 1/2048 | — | 1/2 | $f_{bus}$ |
| 1 | P | SCK Period | $t_{sck}$ | 2 | — | 2048 | $t_{bus}$ |
| 2 | D | Enable Lead Time | $t_{lead}$ | — | 1/2 | — | $t_{sck}$ |
| 3 | D | Enable Lag Time | $t_{lag}$ | — | 1/2 | — | $t_{sck}$ |
| 4 | D | Clock (SCK) High or Low Time | $t_{wsck}$ | — | 1/2 | — | $t_{sck}$ |
| 5 | D | Data Setup Time (Inputs) | $t_{su}$ | 8 | — | — | ns |
| 6 | D | Data Hold Time (Inputs) | $t_{hi}$ | 8 | — | — | ns |
| 9 | D | Data Valid after SCK Edge | $t_{vsck}$ | — | — | 30 | ns |
| 10 | D | Data Valid after $\overline{SS}$ fall (CPHA=0) | $t_{vss}$ | — | — | 15 | ns |
| 11 | D | Data Hold Time (Outputs) | $t_{ho}$ | 20 | — | — | ns |
| 12 | D | Rise and Fall Time Inputs | $t_{rfi}$ | — | — | 8 | ns |
| 13 | D | Rise and Fall Time Outputs | $t_{rfo}$ | — | — | 8 | ns |