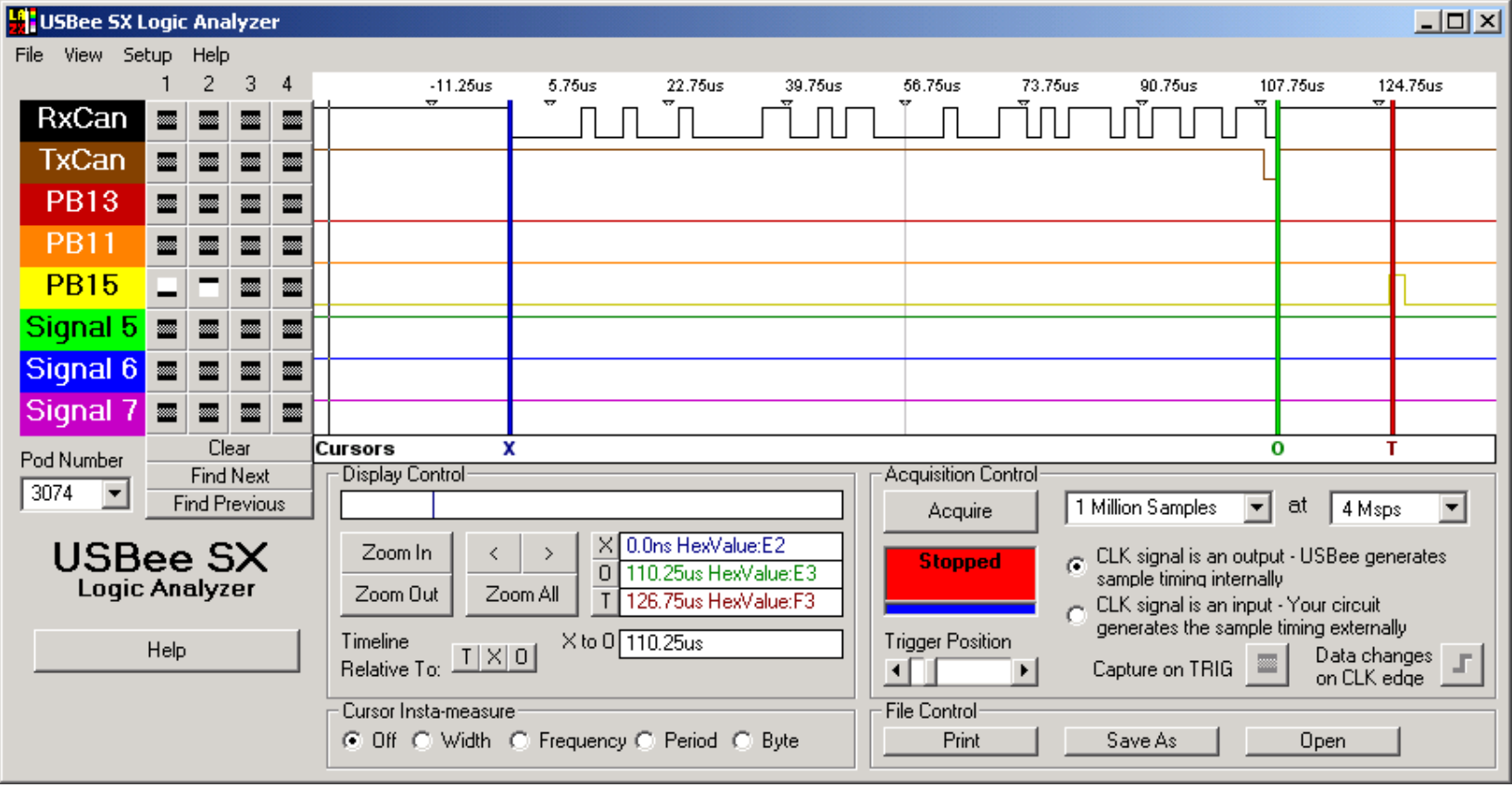
USBee SX Logic Analyzer
File
View
Setup
Help
1
2
3
4
RxCan
TxCan
PB13
PB11
PB15
Signal 5
Signal 6
Signal 7
-11.25us
5.75us
22.75us
39.75us
56.75us
73.75us
90.75us
107.75us
124.75us
Cursors
X
O
T
Clear
Find Next
Find Previous
Pod Number
3074
USBee SX
Logic Analyzer
Help
Display Control
Zoom In
Zoom Out
Zoom All
X 0.0ns HexValue:E2
O 110.25us HexValue:E3
T 126.75us HexValue:F3
Timeline Relative To:
T
X
O
X to O
110.25us
Acquisition Control
Acquire
Stopped
1 Million Samples
at
4 Msps
CLK signal is an output - USBee generates sample timing internally
CLK signal is an input - Your circuit generates the sample timing externally
Trigger Position
Capture on TRIG
Data changes on CLK edge
Cursor Insta-measure
Off
Width
Frequency
Period
Byte
File Control
Print
Save As
Open