

December 9, 1999, 9 am to 12 noon

(15) Question 1. In this problem you will design a frequency meter using input capture, output compare, and interrupt synchronization. The digital signal is connected to PT1. You will also use the timer channel 5. The range of frequencies is 0 to 1000 Hz, and the desired frequency resolution is 0.0625 Hz. You do not need to check for overflow, i.e., you may assume the signal will be less than 1000 Hz.

(5) Part a) unsigned 16-bit binary fixed point with $\Delta = 0.0625$, e.g., $123.375/0.0625=1974$

(10) Part b) change 10 seconds to 16 seconds. Probably should change the name FourHundred to Sixty

```
if (++FourHundred==640){ // take measurement every 16 seconds
    Freq = Count; // 0.0625 Hz units
```

(40) Question 2. In this problem, you will design a blood pressure DAS.

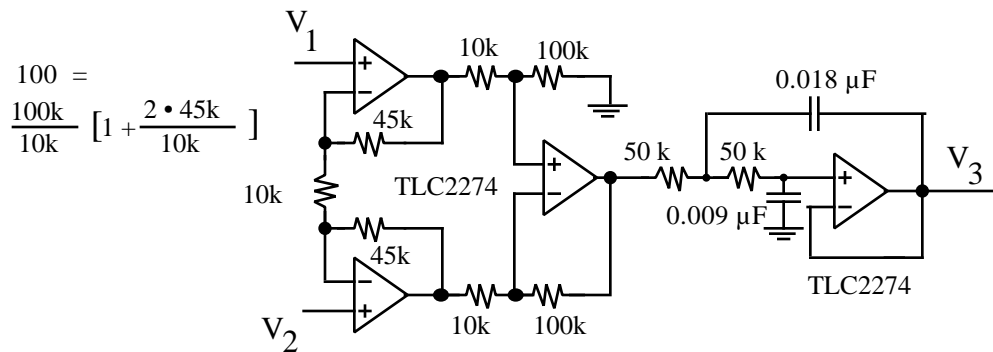
(5) Part a) Complete the following table. Gain needs to be 100.

P	R	R1	R2	R3	R4	V1	V2	V1-V2	V3	ADROH
0	0	1000	1000	1000	1000	2.5	2.5	0	0	0
150	5	995	1005	1005	995	2.5125	2.4875	0.025	2.5	128
300	10	990	1010	1010	990	2.525	2.475	0.05	5.0	255
mmHg						V	V	V	V	

(5) Part b) The sampling rate should be at least 500 Hz, because of the Nyquist Theorem.

(10) Part c) Gain is 100 and LPF at 250 Hz.

- select the cutoff frequency, $f_c = 250$ Hz
- divide the two capacitors by 2
 - $C_{1A} = 141.4\mu F/2 \Rightarrow 141.4\mu F/(2 \cdot 250) = 0.09 \mu F$
 - $C_{2A} = 70.7\mu F/2 \Rightarrow 70.7\mu F/(2 \cdot 250) = 0.045 \mu F$
- resistance scale to get $R = 50$ k . let $x = 5$
 - $R = 10$ k $\cdot x$
 - $C_{1B} = C_{1A}/x = 0.09/5 \mu F = 0.018 \mu F$
 - $C_{2B} = C_{2A}/x = 0.045/5 \mu F = 0.009 \mu F$



(5) Part d) The maximum allowable noise should be less than the resolution at input = $0.05/256=200$ mV

(5) Part e) Show the ritual..

(10) Part f) Show the ISR. The trick to this problem is to implement a MACQ that does not require shifting the data on each sample. To avoid a gadfly loop, the ADC is started at the end of the ISR (could also have used continuous conversion mode, but that would have required more power.)

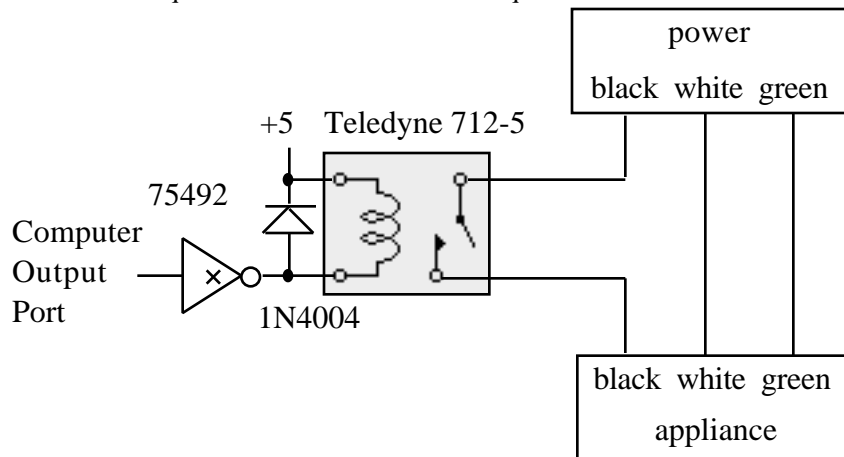
```
#define OC5 0x20
#define fs 500
/* sampling rate in Hz */
#define Rate 2000
/* sampling period in us */
unsigned int index; // index into MACQ represents the current sample
unsigned int x[fs]; // MACQ of 16 bit unsigned pressure samples 0 to 300 mmHg
long sum; // current sum of last 500 samples
unsigned int y; // output of digital LPF, 0 to 300 mmHg
void ritual(void){ unsigned int j;
asm(" sei"); // make atomic
for(j=0;j<fs;j++) x[j]=0;
TIOS|=OC5; // enable OC5
TSCR|=0x80; // enable
```

```

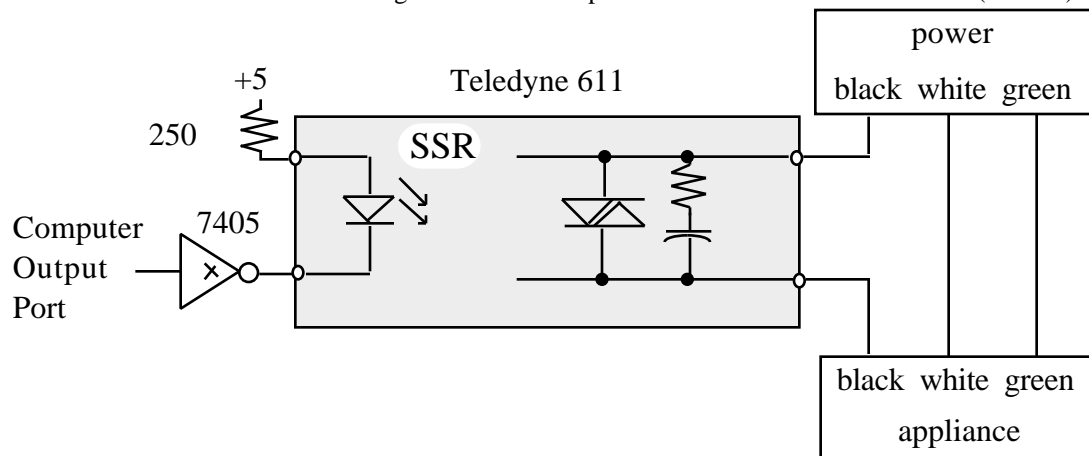
TMSK2=0x33; // 1 us clock
TMSK1|=0C5; // Arm output compare 5
index = 0;
sum=0;
TFLG1=0C5; // Initially clear 0C5F
TC5=TCNT+Rate; // First one in 2 ms
ATDCTL2 = 0x80; // Activate ADC
ATDCTL5=0; // Start A/D, channel 0
asm(" cli"); }
#pragma interrupt_handler TC5handler()
void TC5handler(void){
    TFLG1=0C5; // Ack interrupt
    TC5=TC5+Rate; // Executed every 2 ms
    if(++index == fs) index=0; // wrap
    sum = sum - x[index]; // remove oldest
    x[index]=(ADROH*75+32)>>6; // x[index] is x(n), in mmHg
    sum = sum + x[index]; // add newest
    y=sum/fs; // y(n)=(x(n)+x(n-1)+ + x(n-499))/500
    ATDCTL5=0; // Start A/D for next time, channel 0
}
    
```

(15) Question 3.

(10) Part a) There are two relays described in Chapter 8 that could work. The EM relay (Teledyne 712-5) is cheaper, but the SSR (Teledyne 611) has a longer life. Both automatically provide ground isolation. The EM relay interface is similar to the DC motor. The 50 5V coil needs about 100 mA to activate. A 75492 (also 75451, ULN2074, TIP 120, or IRF540) can sink the required 100 mA. The diode is required to shunt the back EMF.



The SSR interface is similar to a single LED. The set point is +2V 10mA. The resistor is $(5-2-0.5)/0.01 = 250$.

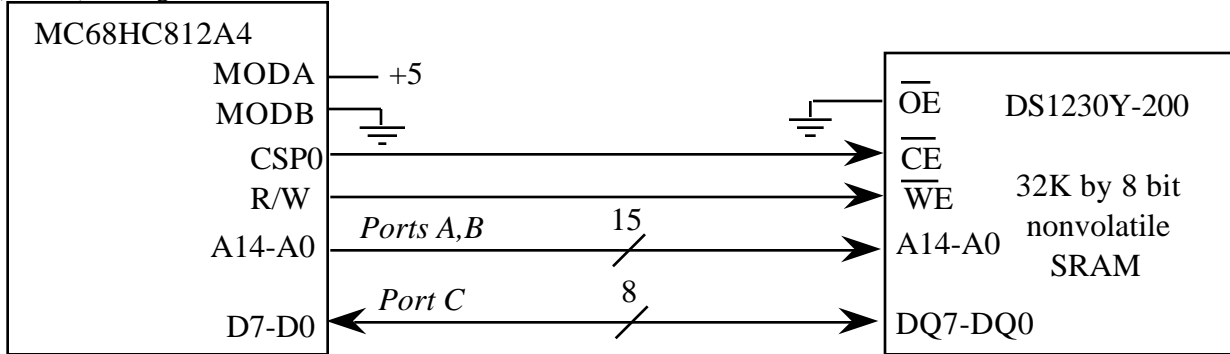


(5) Part b) A **bang-bang controller** uses a relay to affect the physical plant. Other names for the same controller are binary two-position or on-off.

(30) Question 4. interface a DS1230Y-200 32K by 8-bit nonvolatile SRAM to a MC68HC812A4.

(5) Part a) In expanded mode, the EEPROM is initially at \$1000 to \$1FFF, so we place the DS1230Y at \$8000 to \$FFFF, so that there will be a reset vector.

(5) Part b) The digital interface between the DS1230Y-200 and the MC68HC812A4.



$$(5) \text{ Part c) Read Data Available} = (\text{later} (AdV+t_{ACC}, CE+t_{CO}), \text{earlier} (AdN+t_{OH}, CE+t_{OH}))$$

$$= (\text{later} (60+200, 60+200), \text{earlier} (1+20+5, 1+10+5))$$

During a read cycle the data is required by the 6812. Thus to determine the read data required interval, we look in the 6812 data sheet. For read data required, the worst case is the longest interval. Recall that

$$RDR = \text{Read Data Required} = (1 - 11, 1 + 12) = (1 - 30, 1 + 0)$$

We must choose the number of cycle stretches to make the read data available interval overlap the read data required interval. We must make $\overline{W} = 1$ during a read cycle. Thus,

Address	60 + 200	1 - 30	and	1 + 25	1
CE	60 + 200	1 - 30	and	1 + 15	1

First column (290 - 1) tells us that **2 extra cycles** are needed to stretch the access time to 375ns.

(5) Part d) Data is written into the memory when CE=0, and WE=0. During a write cycle, the data is supplied by the 6812. For write data available, the worst case is the shortest interval. Recall that

$$WDA = \text{Write Data Available} = (2 + 13, 1 + 14) = (106, 1 + 20)$$

Since we have chosen to synchronize CE (write cycle 2 in the data sheets),

$$\text{Write Data Required} = (CE - 80, CE + 10)$$

where CE is 1+10. The number of cycle stretches will also affect whether or not the write data available interval overlaps the write data required interval.

$$\text{Thus,} \quad 106 \quad 1+10 - 80 \text{ and} \quad 1+20 \quad 1 + 20$$

$$196 \quad 1$$

Therefore, only **1 cycle stretch** is needed for the write cycle. Two stretches will be used.

(10) Part e) Show the combined read cycle timing diagram. OE=0.

