Jonathan W. Valvano First Name: _______________ Last Name: _____________________

May 15, 1998, 9am-12noon

This is an open book, open notes exam. You may put answers on the backs of the pages, but please don't turn in any extra sheets. You have 3 hours, so please allocate your time accordingly.

(35) Question 1. The objective of this problem is to develop a pressure monitoring system. The signal of interest ranges from DC to 10 Hz. The pressure transducer has a linear response for inputs ranging from 0 to 1000 dynes/cm^2. For this range the output current ranges from 0 to 500 µA. The transducer frequency response is DC to 10 Hz. The 6812 8 bit A/D, 0 to +5 V, will be used.

(20) Part a) Show the analog interface between the transducer output (current) and the A/D input. One tricky part is the conversion from current to voltage. Simply using a resistor to ground to create a voltage from the current is NOT allowed. Convert the full scale pressure signal (0 to 1000 dynes/cm^2) to the full scale (0 to +5 V) A/D input. Include a 2 pole analog active low pass filter with a cutoff frequency of 10 Hz.

(4) Part b) If the signal of interest is 0 to 10 Hz, and the transducer bandwidth is limited to 10 Hz, why was the 10 Hz analog low pass filter required? Give a 1 sentence answer.

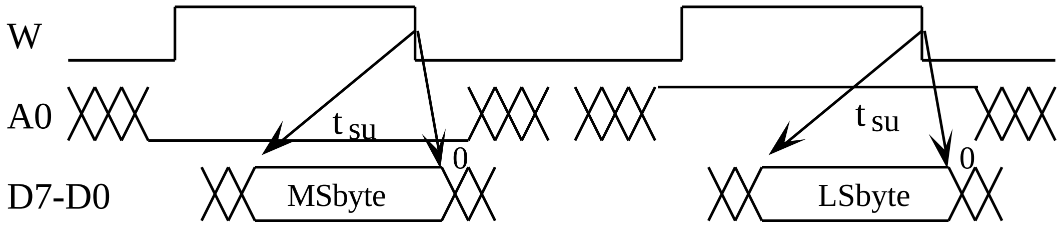
(3) Part c) What is the transducer sensitivity? Show your work and include units in all calculations.

(4) Part d) Normally when considering analog circuit noise, we refer all the possible noise sources to the amplifier input. In this case the amplifier input is a current, so rather in this system, we will refer the analog circuit noise to the amplifier output. What is the maximum allowable voltage noise referred to the amplifier output? Show your work and include units in all calculations.

(4) Part e) What is the system resolution? Show your work and include units in all calculations.

(35) Question 2. Interface a 16 bit D/A converter directly to the MC68HC812A4 address/data bus. Assume the 6812 is running at 8 MHz in expanded narrow mode without cycle stretching. The D/A implements big Endian data format and accepts the most significant byte first (saving it in a latch). When the least significant byte is sent, then entire 16 bit data value is sent to the D/A and the analog output changes. The setup time is t_{su} (to be considered in part g) and the hold time is 0.

W	**A0**	function
0	X	no operation, analog output remains from a previous write
1	0	most significant byte latched from D7-D0 on the fall of **W**
1	1	least significant byte latched from D7-D0 on the fall of **W**, analog output changes



(5) Part a) Design the minimal cost, positive logic address decoder for this device (not all devices in the system.) Show your work including the digital equation for **Select** and the digital logic implementation. Include chip numbers but not pin numbers. The address map is

```
$0000 to $01FF I/O registers
$0800 to $0BFF internal RAM
$0C00 to $0C01 your D/A
$1000 to $1FFF internal EEPROM
$8000 to $FFFF external PROM
```

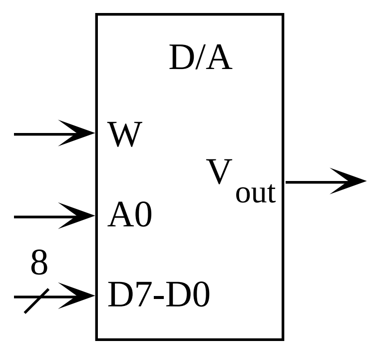
(5) Part b) Give the timing equation for *write data available*. Express your answer is actual ns from the start of the cycle (first fall of the E).

(5) Part c) Give the timing equation for *write data required*. Express your answer as an equation using only the terms like **AdV**, **AdN**, $\mathbf{t_{su}}$, $\downarrow$**W** and $\uparrow$**W**. Don't calculate the actual interval in ns.

(5) Part d) Show the combined table with **Select**, **R/W**, and **E** as inputs and **W** as output, and determine the digital equation for **W**.

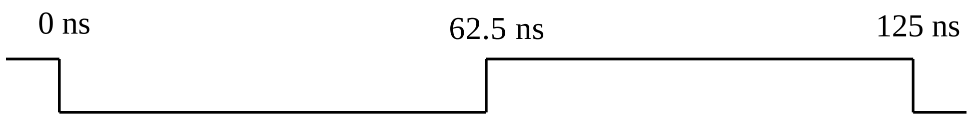
Select	**R/W**	**E**	**W**
0	0	0	
0	0	1	
0	1	0	
0	1	1	
1	0	0	
1	0	1	
1	1	0	
1	1	1	

(5) Part e) Show digital circuit for the interface between the 6812 and the D/A. You do not have to redraw the digital circuit from part a), just label the signal **Select**. Please label TTL chip numbers but not pin numbers.



(5) Part f) Show the combined **write cycle** timing diagram. Assume a 10 ns gate delay through any digital gate. All signals are outputs except Data Required. Use arrows to signify causal relations.

E



R/W

A15-A0

Select

W

Write Data Available

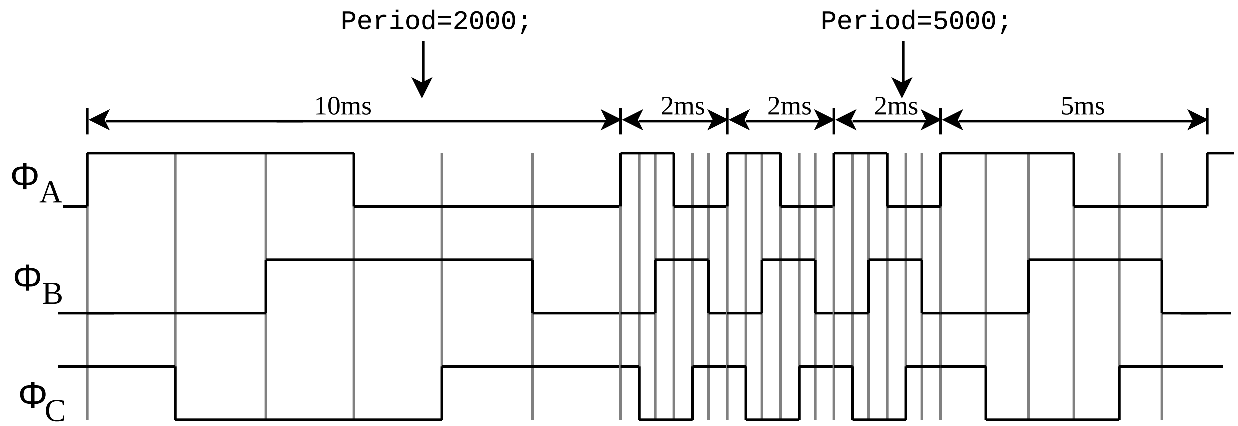
Write Data Required

(5) Part g) What is the maximum allowable setup time, t_{su}, for the D/A. Show your work.

(30) Question 3. You will write software to create a 3-phase digital waveform. You will create three separate digital waveforms (Φ_A, Φ_B, Φ_C), each with the same period, but time shifted by 120° and 240°. The desired period (in µsec) will be stored in a shared global named `Period`. I.e.,

```
unsigned int Period;   // the period in µsec of the ΦA, ΦB, ΦC
```

You may assume `Period` has a maximum value of 65000. The main program will change the period simply by writing to this global, but the waveform will not change until the next rise of Φ_A. In this way, the 0, 120°, 240° phase differences are maintained. In the following example, the initial value of `Period` is 10000. At the first arrow, the software changes the `Period` to 2000, and at the second arrow, the software changes it to 5000.



(5) Part a) What factors determine the minimum allowable value for `Period`? Justify your answer.

(25) Part b) Show the ritual, data structures, and interrupt handlers required to solve this problem. Use comments to define which 6812 signals will become Φ_A, Φ_B, Φ_C. No external hardware is allowed.