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September 29, 2004, 1 to 1:50pm

This is an open book, open notes exam. You may put answers on the backs of the pages, but please don't turn in any extra sheets.

(10) Question 1. An unsigned 8-bit binary fixed-point number system has a Δ resolution of 1/4. What is the corresponding value of the number if the integer part stored in memory is 200?

(10) Question 2. Answer the following questions with reference to a SPI/DAC interface.

Part a) Why was the 6812 selected as the master?

A) Because the DAC was needed to drive the clock
B) So that 8 bits of data could be sent serially
C) In order to satisfy the set up and hold times of the interface
D) Because the 6812 software needed to control when data was to be sent

Part b) What happens if the software selects too fast of a baud rate?

A) The slew rate of the clock would diminish.
B) The 6812 would output incorrect data
C) The DAC would receive incorrect data
D) The SPI/DAC interface works at all baud rates for all DAC chips

Part c) What happens if the CPOL bit is incorrect (w/ CPHA unchanged)?

A) The data bits would be inverted.
B) The data bits would be reversed
C) The setup and hold times would be violated
D) The SPI/DAC interface works for both modes

(10) Question 3. How would you describe this code to acknowledge an output compare 7 interrupt?

```
TFLG1 |= 0x80;  // clear C7F
```

A) It is the proper way to acknowledge the interrupt
B) It doesn't work because it does not clear **`C7F`**
C) It mistakenly clears all the bits in **`TFLG1`**
D) It doesn't work because it is nonreentrant
E) It doesn't work because it sets **`C7F`** rather than clearing it

(15) Question 4. You have a 12-bit 0 to +5V digital to analog converter (DAC) and use it to create an analog output wave. The output rate is 1000 samples/sec. This means a periodic interrupt will output a new value to the DAC every 1 ms.

Part a) What is the expected voltage resolution?

Part b) What is the maximum slew rate (assuming it is limited by the software)?

(25) Question 5. The goal of this problem is to implement the following digital filter. The sampling rate is 1000Hz, and the ADC is a 12-bit signed -5 to +5V range converter.

y(n) = 0.125x(n) + 0.75x(n-3) – 0.625y(n-2)

(10) Part a) Show the fixed-point equation that implements this filter. No floating point is allowed. Choose integer constants that give an exact implementation with the smallest possible single denominator. (no C code, just a fixed-point equation)

(5) Part b) Assuming the input samples are 12-bit signed numbers (-2048 to +2047), what precision is required during the calculation of the filter? In particular circle one of the following options:

`char`
`short`
`long`
`double`

justify your answer.

(10) Part c) Calculate the DC gain of this filter.

(30) Question 6. The objective of this question is to design the analog electronics to interface a transducer to the 0 to +5V built-on ADC of the 6812. The transducer output is a single voltage (relative to ground, not differential), with a range of 1 to 2 volts.

(10) Part a) Derive a linear equation that maps the full-scale transducer output to the full-scale ADC input.

(20) Part b) Build this circuit with one op amp and a REF03 2.50V analog reference. You do not need to show the power connections. You do not need to include an analog low pass filter.