

Jonathan W. Valvano October 21, 1998, 11:00 to 11:50am

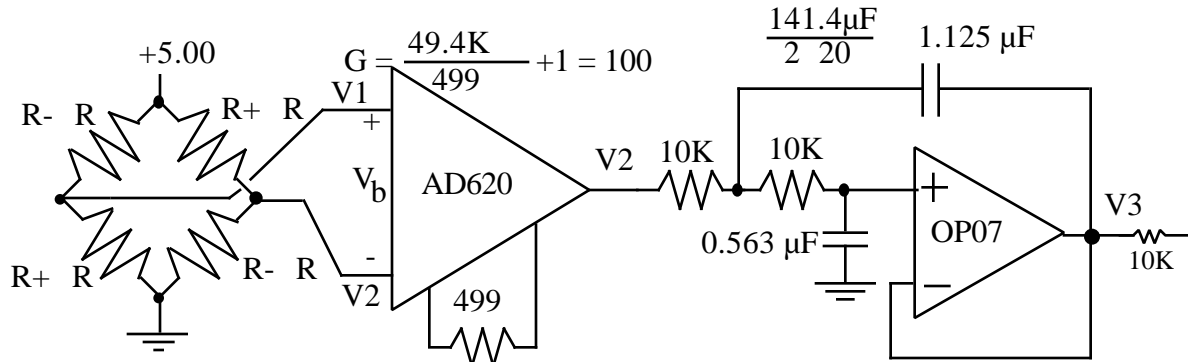
(50) **Question 1.** Design an electronic scale using a 6812.

(10) Part a) What is the bridge output ( $V_1-V_2$ )? What gain is required?

$$V_1 = 5.00 \cdot 101/200 = 2.525V \quad V_2 = 5.00 \cdot 99/200 = 2.475V \quad V_1 - V_2 = 0.05V \quad \text{Gain} = 5/0.05 = 100$$

(15) Part b) Design the pre-amp.

(15) Part c) Design the two pole LPF with a cutoff of 20 Hz.



You could scale the capacitors to standard values 0.1 and 0.2  $\mu\text{F}$  changing the 10K resistors to 56K.

(5) Part d) The system resolution is 1 Kg divided by 256 or 3.9 g.

(5) Part e) The sampling rate should be above 20 Hz because of the Nyquist Theorem.

(50) **Question 2.** The objective of this problem is to interface a SCR (could also use a TRIAC).

(20) Part a) Give the ritual which initializes the interface. You may use any Port T feature.

```
void Init(void) {
```

```
    asm(" sei ");           // make atomic
    TIOS  &= ~0x01;        // PT0 input capture
    DDRT  &= ~0x01;        // PT0 input = Sync signal, interrupt on rise
    TIOS  |= 0x04;         // PT2 output compare
    DDRT  |= 0x04;         // PT2 output = Control signal, delayed 100 us pulse
    TSCR  = 0x80;          // enable TCNT
    TMSK2 = 0x30;          // 125ns clock
    TCTL2 = (TCTL2&0xCF) | 0x20; // PT2 cleared on Output Compare
    TCTL4 = (TCTL4&0xFC) | 0x01; // on rise of PT0
    TMSK1 |= 0x01;         // Arm input capture C0F
    TMSK1 &= ~0x04;        // Disarm output compare C2F
    TFLG1 = 0x05;          // initially clear both C2F and C0F
    T=64000;                // initially power is off
    PORTT&= ~0x04;         // Control=0;
```

```
    asm(" cli ");}
```

(25) Part b) Give the TC2handler() and TC0handler() interrupt handlers.

```
#pragma interrupt_handler TC0handler()
```

```
void TC0handler(void) { // called in rise of Sync
    TFLG1=0x05; // acknowledge, clear both C2F and C0F
    TC2=TC0+T; // delay exactly T cycles from rise of Sync to rise of Control
    TCTL2=(TCTL2&0xCF) | 0x10; // PT2 set on next Output Compare
    TMSK1 |= 0x04; } // Arm output compare C2F
```

```
#pragma interrupt_handler TC2handler()
```

```
void TC2handler(void) { // called exactly T cycles after rise of Sync
    TFLG1=0x04; // acknowledge, clear C2F
    TC2=TC2+800; // delay exactly 800 cycles to fall of Control
    TCTL2 = (TCTL2&0xCF) | 0x20; // PT2 clear on next Output Compare
    TMSK1 &= ~0x04; } // Disarm output compare C2F
```

(5) Part c) The TC0handler() interrupt handler must finish within 300  $\mu\text{sec}$  (2400 cycles) of the rise of Sync. If more than 300  $\mu\text{sec}$  elapses then TCNT will be past  $\text{TC}_2 = \text{TC}_0 + T$ ; (when  $T = 2400$ ) and the clock must go all the way around before the output compare event will occur. Note also that the TC2handler() interrupt handler must finish within 100  $\mu\text{sec}$  (800 cycles) of the setting of C2F.