EE445M/EE380L.6 Quiz1 Spring 2014 Solution

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(10) Question 0. Please staple your crib sheet to your exam. Your crib sheet will be graded on content and correctness.

(5) Question 1. Assume a writer has begun to write. Next a reader enters and blocks on **`wait(&wrt)`**. A second, third, fourth… reader can enter the system and begin reading while the writer is still active.

D) It is now broken, and may allow multiple readers to read at the same time a writer is writing.

(5) Question 2.

Part a) **Stabilize means to fix all the inputs and the times inputs are available so the system can be run over and over, yielding the same outputs each time it is run.**

Part b) **All the main programs where there was no switch input or UART input were examples of stabilization.**

(20) Question 3. Consider a problem of running two foreground threads (**`client`** and **`server`**)

```
Sema4Type InValid; // 1 means In1,In2 are valid, 0 means not valid
Sema4Type OutValid;// 1 means Out is valid, 0 means not valid
```

Initially, both semaphores are 0

```
void client(void){
  Init(); // set up B,D,E ports
  while(1){
    In1=GPIO_PORTB_DATA_R; // read
    In2=GPIO_PORTD_DATA_R; // read
    OS_Signal(&InValid);
    OS_Wait(&OutValid);
    GPIO_PORTE_DATA_R=Out; // write
  }
}
```

```
void server(void){
  while(1){
    OS_Wait(&InValid);
    Out = (In1+In2)/2; // average
    OS_Signal(&OutValid);
  }
}
```

(10) Question 4. Consider this example of two background threads.

Part a) Does this code have a critical section? **No**

Part b) If you do not think it has a critical section, justify your choice with a reason why no critical section exists.

The `cnt` variables, although global, are not shared. Notice one `cnt` is at `0x20000000` and the other at `0x20000004`. Since the globals are not shared there is no critical section.

(20) Question 5. There are three FIFOs like the following, implemented with blocking semaphores.

Part a) Can you choose a FIFO large enough to prevent a deadlock? Justify your answer.

There is no deadlock. Think of the total number of elements in all three FIFOs combined. It starts out with 1 element, each loop removes one element, and then adds an element. So at the end of each loop there is one element, meaning one of the three threads can run. They run in a T1 T2 T3 T1 T2 T3… cyclic order.

Part b) If it can run without deadlock, how large does the FIFO need to be to prevent a deadlock?

Each FIFO needs only one element.

(10) Question 6. The following system uses timer-triggering to sample PE3 at 1000 Hz.

Because this is timer-triggered sampling, there is no time jitter, hence there is no error in the voltage. Notice the higher/equal priority ISRs run with a total of less than 1ms, so no data will be lost. The data shows up in the FIFO at variable times, but the data itself are perfectly sampled. This IS the proper way to sample an ADC.

(20) Question 7. A sleep parameter exists in the TCB, and the preemptive thread switch occurs every Δt.

Part a) What is the minimum and maximum time the thread will actually sleep?

The minimum time will be m*10ms (sleep decrements to zero, and then a SysTick occurs right then)

The maximum time will be m*10ms+(n-1)*Δt (sleep decrements to zero, and n-1 other threads run first)

Part b) What happens to this OS if all threads are sleeping? Will it crash?

It will crash because it spins in the loop with interrupts disabled. Only way out is an NMI interrupt, watchdog interrupt in NMI mode, a hardware reset, or a power-on reset.