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First: \_\_\_\_\_ Last: \_\_\_\_\_

November 20, 2000, 11:00am-11:50am

This is an open book, open notes exam. You must put your answers on these pages only, you can use the back. You have 50 minutes, so please allocate your time accordingly. ***Please read the entire quiz before starting.***

**(40) Question 1.** Implement the following IIR digital filter at 250 Hz. No floating point is allowed.

$$y(n) = 0.375 \cdot x(n) - 0.3125 \cdot x(n-2) + 0.78125 \cdot y(n-2)$$

Every 4 ms, sample ADC channel 2 of the built-in **8-bit** ADC, calculate the IIR filter and output the filter result to Port H. You may assume the filter gain is less than one, so the  $y(n)$  values will be bounded between 0 and 255.

Part a) Show the private global variables required to implement this system.

Part b) Show the ritual that initializes the system. Activate the ADC, set Port H to output, and enable a 250 Hz real time interrupt using output compare channel 0. Initialize data structures as appropriate. The foreground thread, **main**, will call this ritual once, then perform other unrelated tasks, while the ADC sampling operates in the background using output compare interrupts. You do not need to show the main program.

Part c) Show the output compare channel 0 interrupt service routine. Show the code for all functions that you call.

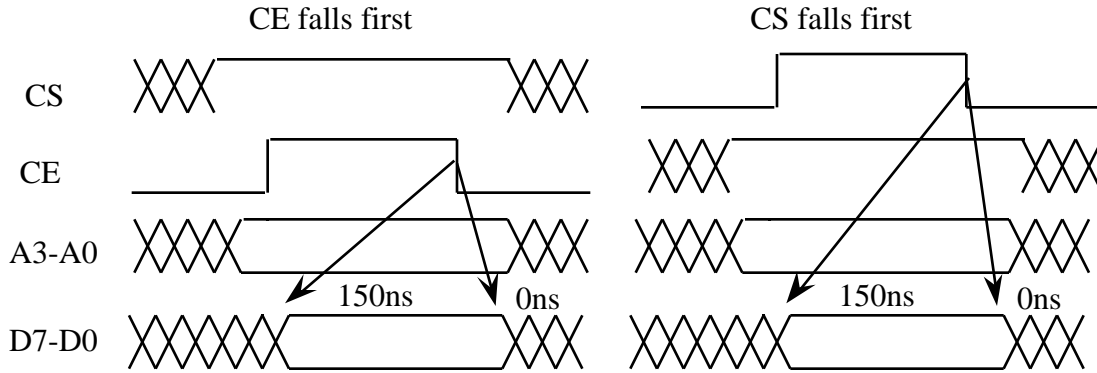
Part d) Show the code that specifies the output compare interrupt vector, i.e., set the 16-bit value at 0xFFEE.

**(20) Question 2.** Design an analog circuit that runs on a single +5V supply. The input range is  $+2 < V_{in} < +3$  V and the output range is  $0 < V_{out} < +5$  V. The input is single ended, i.e., referenced to ground. The output will be connected to the ADC.

Part a) Derive an expression for  $V_{out}$  as a function of  $V_{in}$ .

Part b) Show the circuit. Label all chip numbers, resistors and capacitors but not pin numbers.

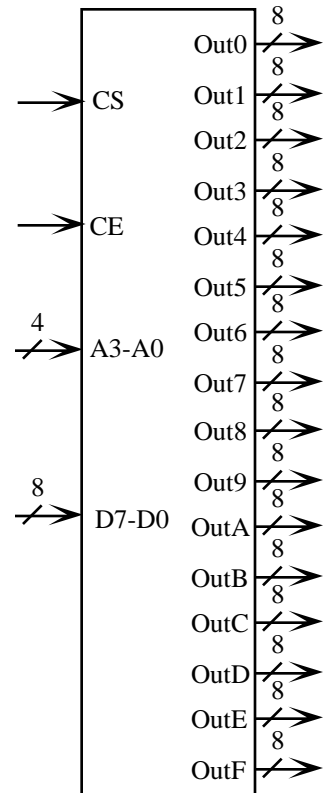
**(40) Question 3.** Interface an Output chip directly to the MC68HC812A4 data bus (not to an output port). The chip is write-only, and your interface should not participate in any read cycles. There are 16 8-bit output ports on the chip. The four address lines A3-A0 determine which one output port is being accessed. Place the Output chip at \$0200-\$020F. For example, a write to 0x0203 will set Out3. Assume an 8 MHz E clock. You will use the CS0 built-in address decoder and choose the proper number of cycle stretches. Assume a 10ns gate delay through each digital gate. When both CE and CS are one, the chip is activated. Whichever CE or CS falls first, causes the 8-bit data to be latched into the chip at the address specified by A3-A0. The setup time is 150ns and the hold time is 0 ns. When either CE or CS is zero, the Output chip ignores the data bus. The two possible timings are:



Part a) What is the write data available interval? Express your answer as a function of the E clock period. Let  $t_{cyc}$  be the E clock period.

Part b) What is the write data required interval? Express your answer as an equation using only the terms like CS and CE. Don't calculate (yet) the actual interval in ns.

Part c) Show digital circuit for the interface between the expanded narrow mode 6812 and the output port. Please label TTL chip numbers but not pin numbers.



Part d) What is the smallest possible number of cycle stretches for this interface? SHOW YOUR WORK.