Exam 1

Date: October 3, 2013

| UT EID: | | |
|---------------------------------|--|---|
| Printed Name: | Last, | First |
| Your signature is on this exam: | your promise that you have not cheated and w | ill not cheat on this exam, nor will you help others to cheat |
| Signature: | | |

Instructions:

- Closed book and closed notes. No books, no papers, no data sheets (other than the last two pages of this Exam)
- No devices other than pencil, pen, eraser (no calculators, no electronic devices), please turn cell phones off.
- Please be sure that your answers to all questions (and all supporting work that is required) are contained in the space (boxes) provided. *Anything outside the boxes will be ignored in grading*.
- You have 75 minutes, so allocate your time accordingly.
- For all questions, unless otherwise stated, find the most efficient (time, resources) solution.
- Unless otherwise stated, make all I/O accesses friendly.
- Please read the entire exam before starting.

| Problem 1 | 10 | |
|-----------|-----|--|
| Problem 2 | 10 | |
| Problem 3 | 10 | |
| Problem 4 | 10 | |
| Problem 5 | 10 | |
| Problem 6 | 15 | |
| Problem 7 | 25 | |
| Problem 8 | 10 | |
| Total | 100 | |

(10) Question 1. State the term that is best described by each definition.

Part a) A last in first out data storage system on the computer used to remember data temporarily.

Part b) Software is added to the system for the purpose of debugging, and this software has a large and significant effect on the system.

Part c) This C operator is used to perform a right shift.

Part d) The name given to describe $1,000 (10^3)$ bytes.

Part e) A type of logic where the voltage representing false is less than the voltage representing true.

Part f) A property of ROM such that data is not lost if power is removed and then restored.

Part g) This addressing mode is always used to access memory, shown here as the source operand of this instruction: LDR R1, [R0]?

Part h) This declaration is used to create a variable in C that has a precision of 8 bits and can take negative values.

Part i) This C operator is used in if-then while-loop and do-while-loops for checking to see if two numbers are not equal.

Part j) A drawing that describes the sequence of operations of software, defining what and when software actions will occur.

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Question 2 (10 points)Consider the following 8-bit subtraction (assume registers are 8 bits wide)Load0xC0 into R1Load0x1F into R2

Subtract R3 = R1-R2

a. What will be the 8-bit result in Register R3 (in hex)?

b. What is 8-bit result in Register R3 (as an unsigned decimal)?

c. What is 8-bit result in Register R3 (as a signed decimal)?

d. What will be the value of the carry (C) bit?

e. What will be the value of the overflow (V) bit?

(10) Question 3. You will fill in the blanks of this C code that initializes Port B. Make pins PB6, PB4, PB1 outputs. Make the pin PB0 an input. To get full credit, this code must be friendly. Partial credit can be obtained by writing code that works, but is not friendly. Mark the box "skip" if it is not required to be executed at that spot in the initialization. You will use the following definitions:



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(10) Question 4. Interface the LED to PB1 such that if PB1 is high, the LED is on, and if PB1 is low the LED is off. The desired LED operating point is 3.0V at 20 mA. The V_{OH} of the microcontroller is 3.1 V. The V_{OL} of the microcontroller is 0.3 V. The maximum current that the microcontroller can source or sink is 8 mA. The V_{OL} of the 7406 is 0.5 V. The maximum current that the 7406 can sink is 40 mA. Your bag of parts includes the switch, the 7406, the LED, and a resistor (you specify the resistor value). Pick the fewest components to use. You will not need them all. You may also use 3.3V, 5V power, and/or ground. Show the equations used to calculate the resistor value.



(10) Question 5. Write an assembly subroutine, called Calc, that calculates Output = (Input/8)-5. The *Input* and *Output* parameters are 8-bit signed numbers located in global RAM. You may use Registers R0-R3, or R12 as scratch registers without saving and restoring them. Full credit will be given to the fastest solution. Don't worry about how *Input* is initialized, just read from *Input* and write to *Output*.

| AREA | DATA, | ALIGN=2 | |
|--------|-------|-------------------|----------------|
| Input | SPACE | 1 | |
| Output | SPACE | 1 | |
| | AREA | .text , CODE, REA | DONLY, ALIGN=2 |

(15) Question 6. Answer the following questions with reference to the C and assembly code below. You may assume that all linkages have been done to be able to call the assembly code from C. <u>Hint</u>: Recall AAPCS

| ; C code calling assembly | ; Assembly code |
|------------------------------|---------------------|
| <pre>int32_t Param1;</pre> | Bs RN 0 |
| <pre>int32_t Param2;</pre> | Res RN 1 |
| int32_t Output; | Ex RN 4 |
| _ | Prod RN 5 |
| <pre>int main() {</pre> | Sub PUSH {R4,R5,LR} |
| Param1 = 2; Param2 = 7; | MOV Ex,#0 |
| Output = Sub(Param1,Param2); | MOV Prod,Bs |
| } | More CMP Prod, Res |
| | BGT Done |
| | MUL Prod, Prod, Bs |
| | ADD Ex, Ex, #1 |
| | B More |
| | Done MOV R0,Ex |
| | POP {R4,R5,LR} |
| | BX LR |

(2) Part a) What is the numerical value in register R0 at the start of the assembly subroutine Sub?

(2) Part b) What is the numerical value in register R1 at the start of the assembly subroutine Sub? R1 =

(4) Part c) What is the numerical value of the C variable Output after the assignment statement,Output = Sub(Param1, Param2); is executed?

output =

(2) Part d) Why did the subroutine Sub, save the registers R4 and R5 on the stack?

- I. The input parameters are on the stack.
- II. The output parameter is returned on the stack
- III. In order to save the return address
- IV. Follows AAPCS convention
- V. None of the above.
- (5) Part e) Which of the following statements describes what Sub does accurately?
 - I. Sub returns the product of the two inputs using successive addition
 - II. Sub returns the largest power to which the first input can be raised and still have it less than or equal to the second
- III. Sub returns the exponent of the first input raised to the second input
- IV. Sub returns the smallest power to which the first input needs to be raised so that it is greater than or equal to the second
- V. Sub returns the power to which the first input has to be raised to be equal to the second

| X ? | | | | | | | |
|------------|--|--|--|--|--|--|--|
| | | | | | | | |
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| | | | | | | | |
| | | | | | | | |
| | | | | | | | |

(20) Question 7. You are asked to develop the software for a control panel of a home automation system. *You can write software in either assembly or C*. Make sure that all of your software is friendly and follows the AAPCS. You may assume the hardware is already connected, and Port B is already initialized so PB5 is an output and PB4–0 are inputs. Please use the port definition GPIO_PORTB_DATA_R to access Port B. You are not allowed to use bit-specific port addressing. The system has five door/window switches (sensors) connected to pins PB4, PB3, PB2, PB1, PB0. Door/window signals are high if OK, and low if there is danger. There is an LED connected to pin PB5, which signifies an alarm. The LED interface is negative logic. Write the main program of the control panel that continuously checks the sensors and turns the warning LED connected if, and only if, two or more door/window switches indicate there is danger.

(10) Question 8. Show the contents of the stack after the two marked points in the execution of the following code. Assume R0=0, R1=10, R2=20, R3=30, R4=40, R5=50, and R6=60. The initial stack pointer is 0x20001008.

```
PUSH {R2,R3}
ADD R4,R1,R0 ; <---- A
POP {R5,R6}
ADD R5,R5,R4
ADD R6,R6,R5
PUSH {R0,R4-R6};
<---- B
```

a) (4 points) The contents of the stack (SP and contents) after execution point A:



b) (6 points) The contents of the stack (SP and contents) after execution point B:



| Me | mory acce | ss inst | ructions | | |
|------|--------------|----------|------------------------------|-----|---|
| | LDR | Rd, | [Rn] | ; | load 32-bit number at [Rn] to Rd |
| | LDR | Rd, | [Rn,#off] | ; | load 32-bit number at [Rn+off] to Rd |
| | LDR | Rd, | =value | ; | set Rd equal to any 32-bit value (PC rel) |
| | LDRH | Rd, | [Rn] | ; | load unsigned 16-bit at [Rn] to Rd |
| | LDRH | Rd, | [Rn,#off] | ; | load unsigned 16-bit at [Rn+off] to Rd |
| | LDRSH | Rd, | [Rn] | ; | load signed 16-bit at [Rn] to Rd |
| | LDRSH | Rd, | [Rn,#off] | ; | load signed 16-bit at [Rn+off] to Rd |
| | LDRB | Rd, | [Rn] | ; | load unsigned 8-bit at [Rn] to Rd |
| | LDRB | Rd, | [Rn,#off] | ; | load unsigned 8-bit at [Rn+off] to Rd |
| | LDRSB | Rd, | [Rn] | ; | load signed 8-bit at [Rn] to Rd |
| | LDRSB | Rd, | [Rn,#off] | ; | load signed 8-bit at [Rn+off] to Rd |
| | STR | Rt, | [Rn] | ; | store 32-bit Rt to [Rn] |
| | STR | Rt, | [Rn,#off] | ; | store 32-bit Rt to [Rn+off] |
| | STRH | Rt, | [Rn] | ; | store least sig. 16-bit Rt to [Rn] |
| | STRH | Rt, | [Rn,#off] | ; | store least sig. 16-bit Rt to [Rn+off] |
| | STRB | Rt, | [Rn] | ; | store least sig. 8-bit Rt to [Rn] |
| | STRB | Rt, | [Rn,#off] | ; | store least sig. 8-bit Rt to [Rn+off] |
| | PUSH | {Rt} | | ; | push 32-bit Rt onto stack |
| | POP | {Rd} | | ; | pop 32-bit number from stack into Rd |
| | ADR | Rd, | label | ; | set Rd equal to the address at label |
| | MOV{S} | Rd, | <op2></op2> | ; | set Rd equal to op2 |
| | MOV | Rd, | | ; | set Rd equal to im16, im16 is 0 to 65535 |
| | MVN {S} | Rd, | <op2></op2> | ; | set Rd equal to -op2 |
| Bra | nch instri | ictions | - | | |
| 210 | B la | abel | ; branch | to | label Always |
| | BEO la | abel | ; branch | if | Z == 1 Equal |
| | BNE la | abel | ; branch | if | z = 0 Not equal |
| | BCS 1a | abel | ; branch | i f | $C == 1$ Higher or same, unsigned \geq |
| | BHS 1a | abel | · branch | if | C == 1 Higher or same unsigned > |
| | BCC 1a | abel | · branch | i f | C == 0 Lower unsigned < |
| | BLO 1a | hal | , branch | if | C == 0 Lower unsigned < |
| | BMT 1a | abel | , branch | if | N = 1 Negative |
| | BDT. 1a | bel | , branch | if | N == 0 Positive or zero |
| | BVS 1a | abel | , branch | if | V == 1 Overflow |
| | BVC 1 | bel | , branch | | V == 0 No overflow |
| | | bel | , branch | | V = 0 NO OVERITOW |
| | | bol | , branch | | $C = 1$ and $Z = 0$ migher, unsigned γ |
| | BCE 1 | bel | , branch | | V = V Crostor than or equal signed > |
| | | bel | , branch | | N V Greater than of equal, signed = |
| | | bel | , branch | | N :- V Less chan, signed < |
| | | bel | ; branch | | Z0 and NV Greater than, Signed > |
| | DIE IC | Der | , branch | | 2-1 of $N = V$ less than of equal, signed 2 |
| | | u bol | ; branch | 10 | arrect to location specified by Rm |
| | | aber | ; branch | | subroutine at label |
| T 4 | | () | ; branch | ĽÖ | subroutine indirect specified by RM |
| Inte | errupt inst | rucuo | ons | | (T-0) |
| | CPSIE | 1 7 | | ; | enable interrupts (1=0) |
| | CPSID | T | | ; | disable interrupts (1=1) |
| | | | | | |
| Log | gical instru | ictions | 3 | | |
| | AND {S} | {Rd, | <pre>} Rn, <op2></op2></pre> | >; | ka=kn&op2 (op2 is 32 bits) |
| | ORR {S} | {Rd, | } Rn, <op2></op2> | >; | Rd=Rn op2 (op2 is 32 bits) |
| | EOR { S } | {Rd, | } Rn, <op2></op2> | >; | Rd=Rn^op2 (op2 is 32 bits) |
| | BIC{S} | {Rd, | } Rn, <op2></op2> | >; | Rd=Rn&(~op2) (op2 is 32 bits) |
| | ORN {S} | {Rd, | } Rn, <op2></op2> | >; | Rd=Rn (~op2) (op2 is 32 bits) |
| | LSR{S} | Rd, | Rm, Rs | ; | logical shift right Rd=Rm>>Rs (unsigned) |

LSR{S} Rd, Rm, #n ; logical shift right Rd=Rm>>n (unsigned) ASR{S} Rd, Rm, Rs ; arithmetic shift right Rd=Rm>>Rs (signed) ; arithmetic shift right Rd=Rm>>n (signed) ASR{S} Rd, Rm, #n LSL{S} Rd, Rm, Rs ; shift left Rd=Rm<<Rs (signed, unsigned) LSL{S} Rd, Rm, #n ; shift left Rd=Rm<<n (signed, unsigned)</pre> **Arithmetic instructions** ADD{S} {Rd,} Rn, $\langle op2 \rangle$; Rd = Rn + op2 $ADD{S} {Rd}, Rn, \#im12$; Rd = Rn + im12, im12 is 0 to 4095 SUB{S} {Rd,} Rn, $\langle op2 \rangle$; Rd = Rn - op2SUB{S} {Rd,} Rn, #im12; Rd = Rn - im12, im12 is 0 to 4095 $RSB{S} {Rd}, Rn, <op2>; Rd = op2 - Rn$ $RSB{S} {Rd_{i}} Rn_{i} \#im12 ; Rd = im12 - Rn$; Rn – op2 CMP Rn, <op2> sets the NZVC bits CMN Rn, <op2>; Rn - (-op2) sets the NZVC bits ; Rd = Rn * RmMUL{S} {Rd,} Rn, Rm signed or unsigned Rd, Rn, Rm, Ra; Rd = Ra + Rn*Rmsigned or unsigned MLA MLS Rd, Rn, Rm, Ra ; Rd = Ra - Rn*Rm signed or unsigned UDIV {Rd,} Rn, Rm ; Rd = Rn/Rmunsigned SDTV {Rd,} Rn, Rm ; Rd = Rn/Rmsigned Notes Ra Rd Rm Rn Rt represent 32-bit registers any 32-bit value: signed, unsigned, or address value if S is present, instruction will set condition codes {S} #im12 any value from 0 to 4095 #im16 any value from 0 to 65535 if Rd is present Rd is destination, otherwise Rn $\{Rd_{\ell}\}$ #n any value from 0 to 31 #off any value from -255 to 4095 any address within the ROM of the microcontroller label the value generated by <op2> op2 Examples of flexible operand **<op2>** creating the 32-bit number. E.g., **Rd = Rn+op2** ADD Rd, Rn, Rm ; op2 = RmADD Rd, Rn, Rm, LSL #n ; op2 = Rm<<n Rm is signed, unsigned ADD Rd, Rn, Rm, LSR #n ; op2 = Rm>>n Rm is unsigned ADD Rd, Rn, Rm, ASR #n ; op2 = Rm>>n Rm is signed ADD Rd, Rn, #constant ; op2 = constant, where X and Y are hexadecimal digits: • produced by shifting an 8-bit unsigned value left by any number of bits in the form **0x00XY00XY** • in the form **0xXY00XY00** in the form **0xXYXYXYX** R0 0x0000.0000 R1 256k Flash R2 **Condition code bits** ROM R3 0x0003.FFFF N negative R4 General R5 Z zero 0x2000.0000 R6 32k RAM purpose -V signed overflow registers **R**7 C carry or 0x2000.7FFF R8 R9 unsigned overflow 0x400<u>0</u>.0000 R10 I/O ports R11 R12 0x400F.FFFF Stack pointer R13 (MSP) Link register R14 (LR) 0xE000.0000 Program counter R15 (PC) Internal I/O PPB 0xE004.1FFF