

This print-out should have 14 questions. Multiple-choice questions may continue on the next column or page – find all choices before making your selection. The due time is Central time.

EE345L Valvano Homework 10.

001 (part 1 of 1) 10 points

What are the possible bus cycle lengths for the MC68HC812A4 running at 8 MHz?

1. Any integer multiple of 125ns
2. 125, 250, 375, and 500ns
3. 250, 500, 750, and 1000ns
4. 125, 250, 500, and 1000ns
5. None of these is correct.
6. 62.5, 125, 187.5, and 250ns

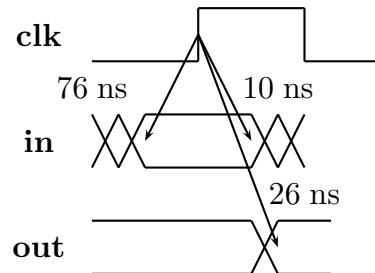
002 (part 1 of 1) 10 points

Which of the following is the best definition of setup time?

1. Setup time is the time before the active edge of a clock that the input data must be valid.
 2. Setup time is the time it takes the output to set up after its input changes.
 3. Setup time is the time after the active edge of a clock that the input data must remain valid.
 4. Setup time is time from enabling the device until the outputs have valid data.
 5. Setup time is the time it takes the device to stabilize after it is initialized.
 6. Setup time is the total length the input data must be valid when writing into a memory.
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003 (part 1 of 1) 10 points

Consider the following timing diagram for a shift register. The rising edge of **clk** shifts one bit from the input **in** into the register. The output of the shift register is available as the signal **out**.

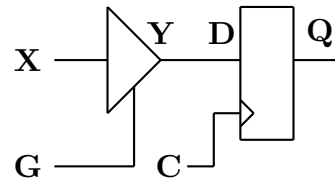


What is the **setup time** for this device? Give your answer in ns.

Answer in units of ns.

004 (part 1 of 3) 10 points

The objective of the system is to transfer the overall input, **X**, to the final output, **Q**. The output of the tristate driver, **Y**, is connected to the data input of the flip flop, **D**.



When the gate signal, **G**, is high, the tristate driver output becomes active, and its output, **Y**, equals its input, **X**. The time from the rise of **G** to the time when **Y** is valid is 17 ns. The time from the fall of **G** to the time when **Y** is invalid is 0. The falling edge of the flip flop clock, **C**, will store its **D** input into the flip flop. In order for the data to be properly saved in the flip flop, its input **D** must be valid 21 ns before the falling edge of **C** and remain valid until 17 ns after that same falling edge of **C**. The value clocked into the flip flop is shown on its output, **Q**.

Which **sequence of actions** will satisfy the objective? The times, **t1** **t2**, will be determined in subsequent questions. The assumption is the sequence can be repeated with no waiting after one sequence, before the next sequence starts.

1. Both signals **G** and **C** are normally low. Make **G=1**, wait **t1**, make **C=1**, wait **t2**, make **G=0**, make **C=0**.

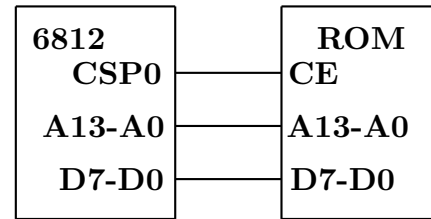
2. Both signals **G** and **C** are normally high. Make **G=0**, wait **t1**, make **C=0**, wait **t2**, make **G=1**, make **C=1**.

3. None of these is correct.

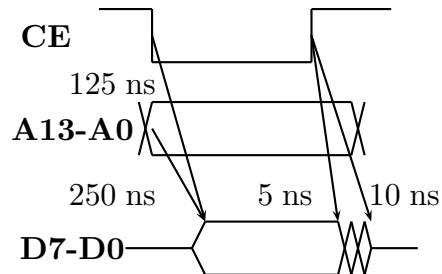
4. The signal **G** is normally low, and the signal **C** is normally high. Make **G=1**, wait **t1**, make **C=0**, wait **t2**, make **G=0**, make **C=1**.

5. All these sequences could work, if the wait times are properly adjusted.

6. The signal **G** is normally high, and the signal **C** is normally low. Make **G=0**, wait **t1**, make **C=1**, wait **t2**, make **G=1**, make **C=0**.



The read cycle timing is described in the following figure,



The ROM data bus floats whenever **CE** is high. 125 ns after the fall of **CE**, and 250 ns after the address is valid the ROM data becomes valid. 5 ns after the rise of **CE** the ROM data becomes invalid. 10 ns after the rise of **CE** the ROM data becomes tristate. What is the fewest number of **cycle stretches** needed to interface this ROM?

1. More than three are needed, so this ROM can not be interfaced.

2. Three cycle stretches are needed.

3. No cycle stretches are needed.

4. One cycle stretch is needed.

5. Two cycle stretches are needed.

005 (part 2 of 3) 10 points

What is the smallest possible value for the time delay, **t1**? Give your answer in ns. Answer in units of ns.

006 (part 3 of 3) 10 points

What is the smallest possible value for the time delay, **t2**? Give your answer in ns. Answer in units of ns.

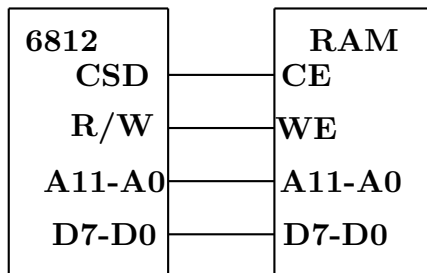
007 (part 1 of 1) 10 points

The objective of this problem is to interface a 16k ROM to the MC68HC812A4 running at 8 MHz. The 6812 **CSP0** is connected to the ROM **CE**. Both **CSP0** and **CE** are negative logic, meaning they are active low. The 6812 data bus signals **D7-D0** are connected to the ROM data lines **D7-D0**. 14 bits of the 6812 address bus signals **A13-A0** are connected to the ROM address lines **A13-A0**.

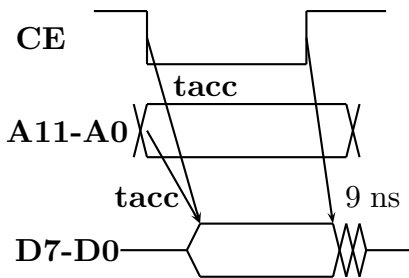
008 (part 1 of 1) 10 points

The objective of this problem is to interface a 4k RAM to the MC68HC812A4 running at 8 MHz. You are given the number of stretches and asked to calculate how fast the memory must be. The 6812 **CSD** is connected to the RAM **CE**. Both **CSD** and **CE** are negative logic, meaning they are active low. The 6812 **R/W** is connected to the RAM **WE**. The 6812 data bus signals **D7-D0** are connected to the RAM data lines **D7-D0**. 12 bits of the

6812 address bus signals **A11-A0** are connected to the RAM address lines **A11-A0**.



The read cycle timing is described in the following figure,



The RAM data bus floats whenever **CE** is high. During a read cycle, let **tacc** be the delay from the fall of **CE** to the time when the data becomes valid. Similarly, let **tacc** be the delay from when the address is valid to the time when the data becomes valid. 9 ns after the rise of **CE** the ROM data becomes invalid. What is the largest value **tacc** can be and still operate with the number of stretches equal to 1? Give your answer in ns.

Answer in units of ns.

009 (part 1 of 2) 10 points

In this problem you are interfacing a RAM to the MC68HC812A4 running at 8 MHz. Assume you are running with the number of stretches equal to 1. Define the start of the bus cycle, which is the falling edge of **E**, to be 0 ns. When does the **Write Data Available** interval start? Give your answer as a decimal number in ns.

Answer in units of ns.

010 (part 2 of 2) 10 points

When does the **Write Data Available** interval end? Give your answer as a decimal number in ns.

Answer in units of ns.

011 (part 1 of 2) 10 points

In this problem you can assume that **DPAGE** is active on the MC68HC812A4, and there is a 1 Mbyte RAM interfaced using **CSD** logic. The goal is to clear the memory location 494748. This memory address is given in unsigned decimal, not hexadecimal. The following C code will be used

```
DPAGE = xxx;
*(char *)yyy = 0;
```

What value should you use in the **xxx** position. Give your answer as an unsigned decimal number.

012 (part 2 of 2) 10 points

What value should you use in the **yyy** position. Give your answer as an unsigned decimal number.

013 (part 1 of 2) 10 points

In this problem you can assume that **PPAGE** is active on the MC68HC812A4, and there is a 4 Mbyte ROM interfaced using **CSP0** logic. The goal is to read the memory location 326978. This memory address is given in unsigned decimal, not hexadecimal. **data** is an 8-bit variable. The following C code will be used

```
PPAGE = xxx;
data = *(char *)yyy;
```

What value should you use in the **xxx** position. Give your answer as an unsigned decimal number.

014 (part 2 of 2) 10 points

What value should you use in the **yyy** position. Give your answer as an unsigned decimal number.