

This print-out should have 11 questions. Multiple-choice questions may continue on the next column or page – find all choices before making your selection. The due time is Central time.

EE345L Valvano Homework 6.

001 (part 1 of 1) 10 points

What is the data packet size in bits used by the SPI? In other words, when one transmission sequence occurs, how many bits are sent?

Answer in units of bits.

002 (part 1 of 1) 10 points

Assume the SPI is configured to run at a frequency of 0.125 MHz. How many microseconds does it take to transmit one packet of information?

Answer in units of usec.

003 (part 1 of 1) 10 points

Which bit turns on the SPI hardware?

1. MSTR
2. SPIE
3. SSOE.
4. CPHA
5. SPE
6. CPOL
7. SPIF

004 (part 1 of 1) 10 points

Assume you wish to interface a slave device to your 6812 using SPI. Assume CPHA will be zero. The slave device shifts the data in on the falling edge of the clock. Which configuration mode should you select?

1. CPOL=1, MSTR=1.
2. CPOL=0, MSTR=0
3. CPOL=1, MSTR=0

4. CPOL=0, MSTR=1

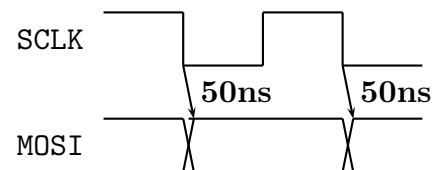
005 (part 1 of 1) 10 points

Which of the following statements best describes the action that will clear the **SPIF** bit in the SPI status register on the 6812?

1. The slave automatically clears the **SPIF** bit.
2. The software writes a 0 to the **SPIF** bit.
3. The software writes a 1 to the **SPIF** bit.
4. The software reads the SPI data register.
5. The 6812 SPI hardware automatically clears the **SPIF** bit after the transmission is complete.
6. The software reads the status register when the the **SPIF** bit is a one, followed by the software reading the SPI data register.

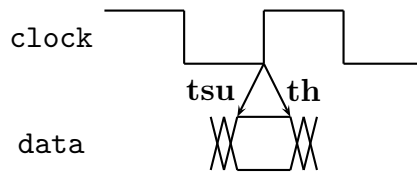
006 (part 1 of 3) 10 points

The following figure shows the timing as one bit is transmitted out of the SPI. In this example, the SPI clocks data out on the falling edge of **SCLK**. The new data on **MOSI** becomes available 50ns after each falling edge.



The following figure shows the timing of the slave device. Both the clock and data are inputs. The data is clocked into the slave on the rising edge of the clock. The setup time, t_{su} , is defined to be the time before the clock the input data must stable. The hold time, t_h , is defined to be the time after the clock the input data must continue to be stable. In other words, the input data must be stable

from t_{su} before the rising edge up to t_h after the `clock`. Conversely, if the input were to change during this must be stable interval then garbage will be clocked in.



How should the 6812 SCLK be interfaced to the slave `clock` input?

1. The SPI SCLK should be connected to the slave `clock` through an open collector driver gate.
2. Both the SPI SCLK and the slave `clock` should be connected to a square-wave oscillator.
3. The SPI SCLK should be connected to the slave `clock` through a logic inverter.
4. The SPI SCLK should be connected directly to the slave `clock`.
5. The SPI SCLK should be connected to the slave `clock` through a tristate driver gate.

007 (part 2 of 3) 10 points

How should the 6812 be interfaced to the slave `data` input?

1. The SPI MOSI should be connected directly to the slave `data`.
2. The SPI MOSI should be connected to the slave `data` through an open collector driver gate.
3. The SPI MISO should be connected to the slave `data` through an open collector driver gate.
4. The SPI MISO should be connected directly to the slave `data`.

5. The SPI MISO should be connected to the slave `data` through a logic inverter.

008 (part 3 of 3) 10 points

Assume the setup time, t_{su} , is 12750 ns. Assume the hold time, t_h , is 6400 ns. The following choices are available for the serial clock frequency, 4, 2, 1, 0.5, 0.25, 0.125, 0.0625 or 0.03125 MHz. Which is the fastest frequency that can be used? Give your answer in MHz.

Answer in units of MHz.

009 (part 1 of 1) 10 points

Assume the DAC precision is 10 bits, and the range is from 0 volts to 5 volts. What is the resolution of this DAC? Give your answer in volts.

Answer in units of volts.

010 (part 1 of 1) 10 points

Assume the DAC range is from 0 to 10 volts. The desired resolution for this DAC is 0.01953 volts. How many bits are needed? Round your answer to the closed whole number. Give your answer in bits.

Answer in units of bits.

011 (part 1 of 1) 10 points

A **stepper motor** has 100 steps per rotation. If this four-step output sequence is repeated over and over

...,9,10,6,5,9,10,6,5,...

and a new output is sent every 10ms, then the **stepper motor** will spin counterclockwise at 60 rpm. What happens if this sequence

...,1,5,4,6,2,10,8,9,1,5,4,6,2,10,8,9,...

occurs such that a new output is sent every 10ms?

1. The motor will spin counterclockwise at 30 rpm.
2. The motor will not spin at all.
3. none of these choices is correct.
4. The motor will spin counterclockwise at

120 rpm.

5. The motor will spin clockwise at 60 rpm.
6. The motor will spin counterclockwise at 60 rpm.
7. The motor will spin clockwise at 30 rpm.
8. The motor will spin clockwise at 120 rpm.