

This print-out should have 12 questions. Multiple-choice questions may continue on the next column or page – find all choices before making your selection. The due time is Central time.

EE345L Valvano Homework 9.

001 (part 1 of 1) 10 points

A serial port is configured to run at a baud rate of 300 bits/sec. The protocol is 8 bit data, 1 stop, and no parity.

What is the bandwidth of this port in bytes/sec?

Answer in units of bytes/sec.

002 (part 1 of 1) 10 points

A serial port can be configured to run at any of the standard baud rates of 300, 600, 1200, 2400, 4800, 9600, 19200, or 38400 bits/sec. The protocol is 8 bit data, 1 stop, and no parity. The system specifications require that data should be transmitted with a bandwidth up to 108 bytes/sec. In order to be able to pass information at this rate, you have to initialize the serial channel to operate at a bandwidth faster than 108 bytes/sec.

What is the slowest allowable baud rate for this serial port in bits/sec?

Answer in units of bits/sec.

003 (part 1 of 1) 10 points

A serial port should be configured to run at the baud rate of 300 bits/sec. The protocol is 8 bit data, 1 stop, and no parity. Assume the 6812 E clock, P clock and M clock are all 8 MHz.

```
ldd    #???
std    SC0BD
```

What 16-bit value should be written into the **SC0BD** register?

004 (part 1 of 1) 10 points

Which of the following statements best describes the action that will set the **RDRF** bit in the **SC0SR1** register on the 6812?

1. The software writes a 1 to the **RDRF** bit in the **SC0SR1** register.

2. None of these choices is correct.

3. The receive shift register contains new input data.

4. The software reads the **SC0SR1** register when the **RDRF** bit is a one, followed by the software reading the **SC0DRL** register.

5. The receive shift register is busy, currently receiving a new input.

6. The receive hardware is idle, ready to receive another input.

7. The receive data register, **SC0DRL**, contains new input data.

005 (part 1 of 1) 10 points

Which of the following statements best describes the action that will clear the **RDRF** bit in the **SC0SR1** register on the 6812?

1. The receive shift register contains new input data.

2. The software writes a 0 to the **RDRF** bit in the **SC0SR1** register.

3. The software writes a 1 to the **RDRF** bit in the **SC0SR1** register.

4. The software reads the **SC0DRL** register.

5. The receive data register, **SC0DRL**, contains new input data.

6. The software reads the **SC0SR1** register when the **RDRF** bit is a one, followed by the software reading the **SC0DRL** register.

7. None of these choices is correct.

006 (part 1 of 1) 10 points

Which of the following statements best describes the action that will set the **TDRE** bit in the **SC0SR1** register on the 6812?

1. The software writes a 1 to the **TDRE** bit in the **SC0SR1** register.
2. The transmit shift register is busy, currently sending a new input.
3. The transmit shift register finishes outputting the last data.
4. The software reads the **SC0SR1** register when the **TDRE** bit is a one, followed by the software writing new data to the **SC0DRL** register.
5. The transmit data register, **SC0DRL**, contains no data. It is empty.
6. None of these choices is correct.
7. The transmit shift register, contains no data. It is empty.

007 (part 1 of 1) 10 points

Which of the following statements best describes the action that will clear the **TDRE** bit in the **SC0SR1** register on the 6812?

1. The transmit shift register, contains no data. It is empty.
2. The transmit data register, **SC0DRL**, contains no data. It is empty.
3. The transmit shift register finishes outputting the last data.
4. None of these choices is correct.
5. The software writes data to the **SC0DRL** register.
6. The software reads the **SC0SR1** register when the **TDRE** bit is a one, followed by the software writing new data to the **SC0DRL** register.
7. The software writes a 0 to the **TDRE** bit in the **SC0SR1** register.

008 (part 1 of 1) 10 points

Which answer best describes the voltage protocol used in **RS232** communication?

1. A logic high (true) is encoded as +5 V, while a logic low (false) will be 0 V.
2. A logic high (true) is encoded as -12 V, while a logic low (false) will be +12 V.
3. A logic high (true) is encoded as +12 V, while a logic low (false) will be 0 V.
4. A logic high (true) is encoded as +12 V, while a logic low (false) will be -12 V.
5. None of these choices is correct.
6. A logic high (true) is encoded as 0 V, while a logic low (false) will be +12 V.
7. A logic high (true) is encoded as 0 V, while a logic low (false) will be +5 V.

009 (part 1 of 1) 10 points

What does it mean for a serial communication system to be **asynchronous**?

1. None of these is correct.
2. The transmitter and receiver operate on physically different clocks, but the two clocks have similar frequencies.
3. The bits are transmitted one at a time.
4. The transmitter and receiver operate on the same clock, but the master generates the clock and the receiver uses it.
5. Communication can occur in both directions but only one direction at a time.
6. Communication can occur in both directions simultaneously.

010 (part 1 of 1) 10 points

What does it mean for a serial communication system to be **half duplex**?

1. The transmitter and receiver operate on physically different clocks, but the two clocks have similar frequencies.
2. Communication can occur in both directions simultaneously.
3. Communication can occur in both directions but only one direction at a time.
4. None of these is correct.
5. The bits are transmitted one at a time.
6. The transmitter and receiver operate on the same clock, but the master generates the clock and the receiver uses it.

rate of 1080 bits/sec. The input channel is configured to generate a SCI interrupt whenever **RDRF** is set. Input latency is defined as the time delay from when new input is ready (**RDRF** is set) and when the software reads the new input. The protocol is 8-bit data, 1 stop, and no parity. What is maximum latency requirement for this real time interface in order to prevent overrun errors? Give your answer in usec.

Answer in units of usec.

011 (part 1 of 1) 10 points

The following is a simple SCI ISR using Metrowerks.

```
unsigned char data;
interrupt 20 void SCIhandler(void){
    if(SCISR1 & 0x80){
        data = SCIDRL;
    }
}
```

Into which memory location is the 16-bit address of `SCIhandler` stored?

1. 0xFFE6.
2. 0xFFD4.
3. None of these is correct.
4. 0xFFD6.
5. 0xFFFF0.
6. 0xFFFFE.
7. 20.

012 (part 1 of 1) 10 points

A serial port is configured to run at a baud