

Lab 1c PCB layout of RAM interface

This laboratory assignment accompanies the book, Embedded Microcomputer Systems: Real Time Interfacing, by Jonathan W. Valvano, published by Brooks-Cole, copyright © 2000.

- Goals**
- To interface a 128K by 8-bit RAM,
 - To layout a PCB board.
- Review**
- Valvano Chapter 9 on interfacing to the MC68HC812A4,
 - Data sheets on the 128K by 8 bit static RAM (same as K6T1008C2E).

Starter files Lab1prep.sch Lab1prep.pcb

Background

You will use the CAD program **ExpressPCB** to layout a 128K by 8-bit RAM interface. The 17-bit RAM address should be connected to the 6812 address bits A16-A0. The 6812 extended address pin **A16** can be found as **PG0**. The 8-bit RAM data (labeled **I/O** in Figure 1.1) should be connected to the 6812 data bits **D7-D0**. The RAM power pin **VCC** should be connected to +5V, while **VSS** is ground. A bypass capacitor, with a value of 0.01 to 0.1 μ F should be placed between power and ground. The RAM pin **CS2** should be connected to +5V. The RAM write enable (**/WE**) should be connected to the 6812 **R/W**. The RAM output enable (**/OE**) should be grounded. The layout will provide for the flexibility of allowing the RAM chip select (**/CS1**) to be connected to either the 6812 **/CSD** or the 6812 **/CSP0**. To use the chip to store data the **/CSD** chip select will be used. On the other hand, to use the chip to store programs the **/CSP0** chip select will be used. The software to activate the interface, hardware construction, and device testing will be performed in a later lab.

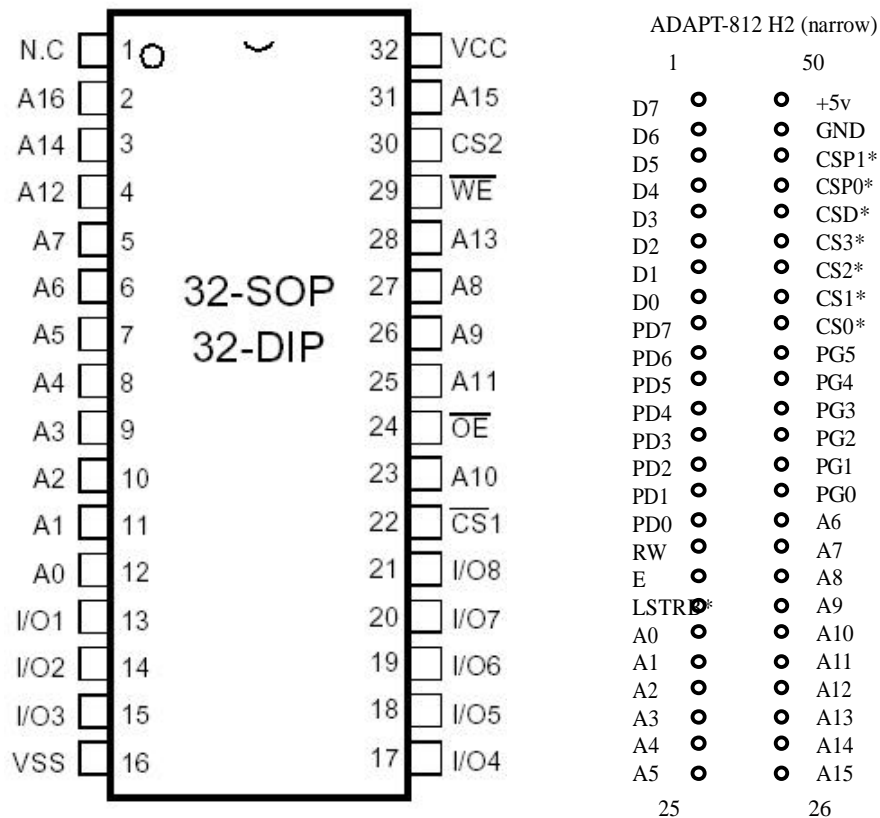


Figure 1.1. Pin locations for the 128K RAM and the 6812 running in expanded narrow mode.

Preparation (do this before your lab period)

Begin by drawing a circuit diagram of the memory interface on the computer using any CAD software. One possibility is to use the **ExpressSCH** CAD drawing program (see starter file **Lab1prep.sch**). Label pin numbers on the 50-pin H2 connector as well as the 32-pin RAM chip. Next, layout the circuit using the **ExpressPCB** program (see starter file **Lab1prep.pcb**). Please read the instructions included in **ExpressPCB** help menu. View the "Tips for Making PC Boards" page at <http://www.expresspcb.com>.

Add labels for your initials, the date, and the purpose of the board,

Place all components on the top side,

If possible align all chips in the same direction,

Configure the board so that all soldering occurs on the bottom side,

Add labeling to the top side to assist in construction and debugging,

Add test points at strategic points to assist in debugging (e.g., power, /CS1, /WE, and ground),

Each IC should have a bypass capacitor, placed as close to the chip as possible,

All components need labels (e.g., U1 R1 C1 J1), shown both on the board and the circuit diagram,

Avoid 90-degree turns, convert them to two 45 degree turns,

After the circuit is done, cover the unused area on the bottom side with a ground plane.

Every lab group will produce an independent circuit diagram and layout as part of the preparation. You must select the MiniBoard service, which creates three identical 3.8 by 2.5 inch boards for \$59. Add features such as test points and labels that will make it easy to test the hardware. Please print out this initial layout and turn it in along with the regular circuit diagram.

Procedure (do this during your lab period)

Then, the lab groups will be combined so that three groups form a layout team. The layout team will meet and integrate the three individual layouts into a single final layout. Again using the simple layout program provided by **ExpressPCB**, create the final layout for the layout team. Please print out this final layout and turn it in to the TA for approval and manufacture. **ExpressPCB** will make three identical PC boards, one for each lab group.

Deliverables (exact components of the lab report)

A) Objectives (1/2 page maximum)

B) Hardware Design

Regular circuit diagram (must be prepared on the computer using any CAD program)

PCB layout and three printouts (top, bottom and combined)

C) Software Design (none)

D) Measurement Data (none)

E) Analysis and Discussion (none)

Checkout (show this to the TA)

none

Hints:

1) The memory will function properly with any connection between the RAM and 6812 address pins, as long as each of the 17 6812 address pins is connected to a separate RAM address pin.

2) The memory will function properly with any connection between the RAM and 6812 data pins, as long as each of the eight 6812 data pins is connected to a separate RAM data pin.

3) The Miniboard service does not produce the silk layer, but you may still wish to use it to help document the design.

4) /CSD and CSD* are two equivalent ways to specify the signal is negative logic

5) Be sure to use the narrow expanded mode of **H2** to locate the 6812 pins.