21.8 A 114GHz VCO in 0.13μm CMOS Technology

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A D-band (110 to 170GHz) CMOS push-push VCO is presented in this paper. Implemented in standard 0.13μm CMOS technology, the VCO has a 114GHz output signal with a phase noise of –107.6dBc/Hz at 10MHz offset, and a power consumption of 8.4mW from a 1.2V supply.

Millimeter wave (MMW) VCO design is motivated by the need for the ever-increasing frequency and bandwidth of communication applications. Most previously reported W-band (75 to 110GHz) and D-band (110 to 170GHz) VCOs are realized in InP HEMT or HBT technology [1-3] due to excellent transistor performances. Recently, some millimeter-wave Si-based VCOs were reported with high power consumption [5-9]. In this paper, a VCO topology based on CMOS technology for MMW applications with low power consumption is proposed. This MMIC is implemented in commercial 0.13μm 1P8M CMOS process with f_T of 85GHz and f_{max} of 90GHz.

Frequency sources can be implemented as fundamental oscillator, VCO-multiplier, or push-push VCO [2]. Due to the advantage of compact chip size and exploiting the higher device gain and passive component and varactor Q-factors available at lower frequencies [2], push-push VCO is more attractive for MMW VCO design. Some reported MMW VCOs are based on cross-coupled topology because of the ease of design [4-5]. However, the cross-coupled topology does not exhibit design flexibility and cannot provide sufficient negative resistance for high frequency oscillation. A topology using two cascaded emitter followers is proposed to overcome this disadvantage [6]; but it suffers from higher supply voltage, and is only suitable in HBT due to the inherent low g_m of CMOS devices. In this paper, the proposed VCO topology based on CMOS technology provides sufficient negative resistance at frequencies where cross-coupled topology cannot provide negative resistance at the same bias condition. Thus the oscillation frequency can be higher with low DC power.

The proposed push-push VCO topology is shown in Fig. 21.8.1. This topology can be separated into two parts. The transistors M_1, M_2 with common-gate inductive feedback (L_g) and source capacitive feedback (C_s, L_s) provide negative resistance to compensate for the loss of passive elements. The inductors (L_{d1}, L_{d2}) implemented with transmission lines and varactors (C_{var1}, C_{var2}) are the parallel LC-tanks. The parallel C_s and L_s source resonator helps devices generate large negative resistance even at frequencies where the CMOS cannot provide enough gain to generate negative resistance. This is due to the fact that when the source resonator has a resonance frequency below the oscillation frequency band, the source resonator exhibits a capacitive reactance for positive feedback in the oscillation frequency. Thus, sufficient negative resistance can be generated. This topology also provides design flexibility to obtain desired frequency response of negative resistance by properly selecting the values of L_g, C_s, and L_s. As shown in Fig. 21.8.2, the local minimum of the frequency response of the negative resistance is designed around 57GHz where the negative resistance is –100Ω. This sufficient negative resistance in the desired frequency band ensures oscillation of the circuit. To excite the push-push signal, the oscillator should operate in odd mode with even mode suppressed.

The transistor size (M_1, M_2) has 6 gate fingers and total gate width of 12μm. The MOS varactors are laid out as multi-fingers to reduce gate resistance. The inductors are realized with transmission lines. To minimize the chip size, the thin-film microstrips are used to implement the reactive elements since it is easier to layout compact meanders compared with CPWs. In this process, the thin-film microstrip line of 50Ω characteristic impedance is about 10μm wide. The L_g, L_d, L_s are optimized as 2.5μm width line (Z_o=92Ω) for physical length and quality factor. The supply voltage is fed through 114GHz quarter-wavelength short stub and the bias current drifts through L_s to ground.

This CMOS VCO is measured via on-wafer probing. The VCO starts to oscillate at a bias current of 2mA at 0.7V. Figure 21.8.3 shows the measured output frequency and power versus the control voltage. With the coarse tuning (V_G), the frequency tuning range at fundamental port is 56.4 to 57.6GHz, and at push-push port is 112.8 to 115.2GHz. The measured output spectrum of push-push port is shown in Fig. 21.8.4. After calibrating the waveguide and probes loss, the measured output power is –5dBm at fundamental port of 57GHz and better than -22.5dBm at push-push port of 114GHz. The fundamental rejection at push-push port is better than 15dB. The core power consumption is 8.4mW with 7mA from a 1.2V supply, and the output buffers consume 12mW. Figure 21.8.5 shows that the measured phase noise of 56.7GHz is –113.6dBc/Hz at 10MHz offset, and the phase noise at the push-push port is expected to be 6dB higher. Summary of measured performance and comparison with recently reported Si-based MMW VCOs are shown in Fig. 21.8.6, and the die micrograph of the fabricated chip is shown in Fig. 21.8.7 with a size of 0.42×0.48mm^2, including RF testing pads.

The development of the 114GHz push-push CMOS VCO is discussed. Since this CMOS VCO has fundamental oscillation at 57GHz, it also has potential for unlicensed 60GHz application.

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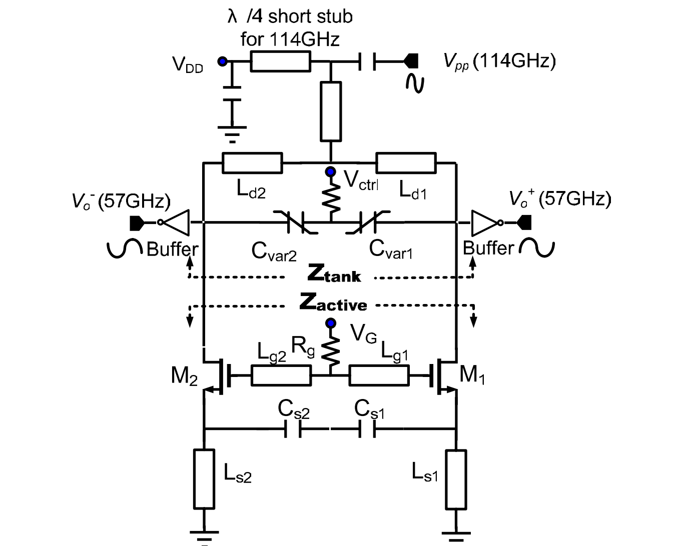

Figure 21.8.1: Schematic of the D-band CMOS VCO.

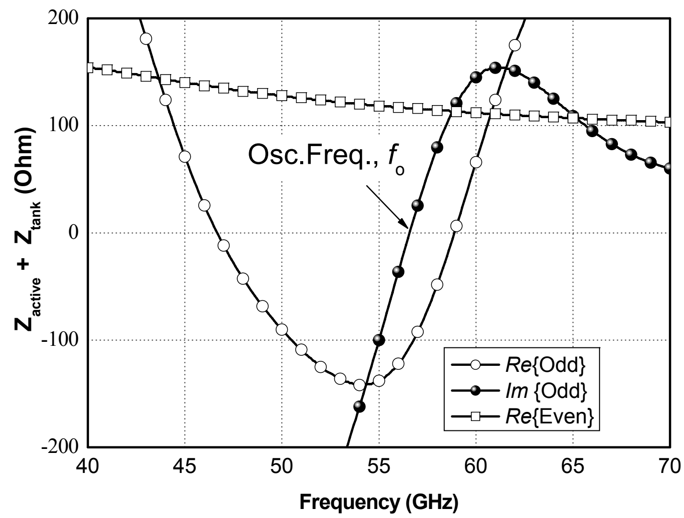

Figure 21.8.2: Small signal start-up oscillation condition of the odd-mode operation with even mode suppressed.

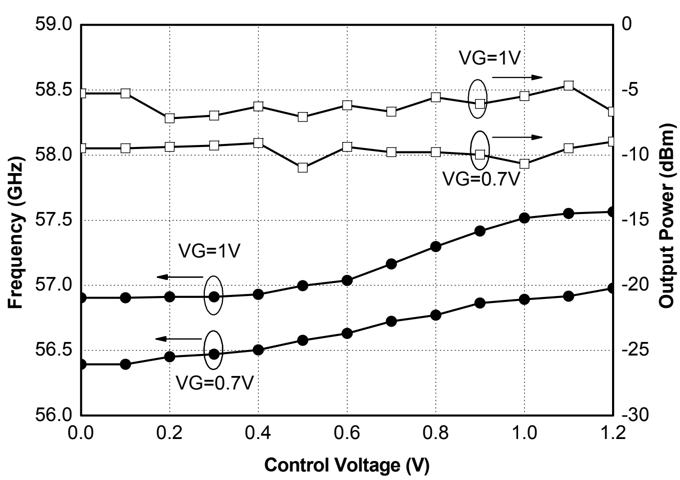

Figure 21.8.3: Fundamental output frequency and power versus control voltage from 0 to 1.2V.

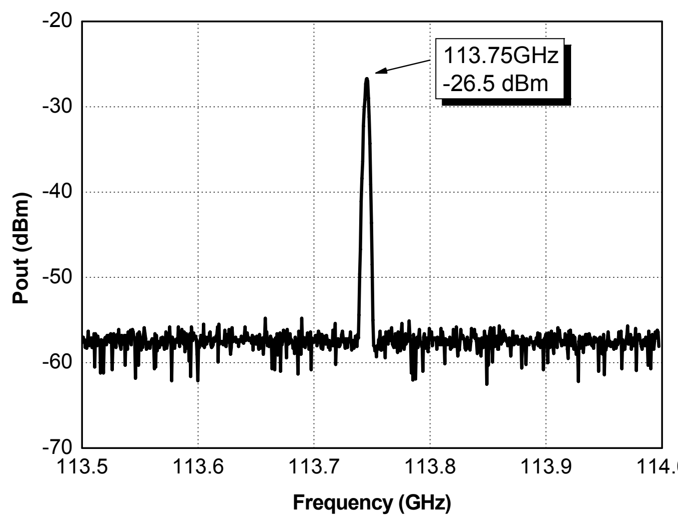

Figure 21.8.4: Measured output spectrum at push-push port before calibration of WG and probes losses.

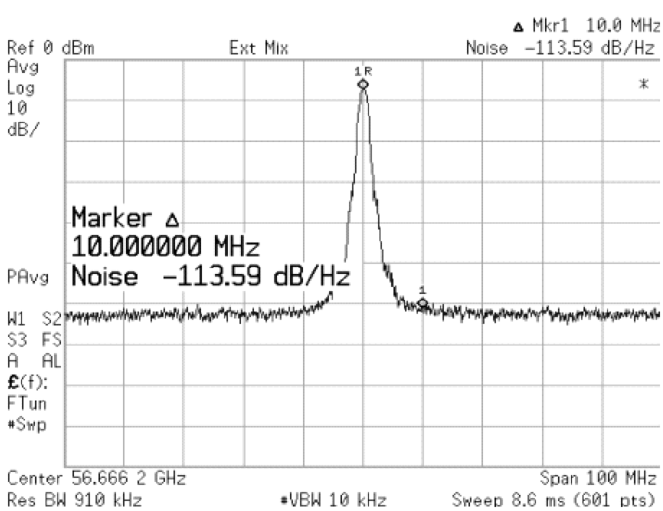

Figure 21.8.5: Measured phase noise at fundamental port.

Process	Frequency (GHz)	Power Supply (V)	Core Power Diss. (mW)	Phase Noise (dBc/Hz)	Offset (MHz)	FOM* (dBc/Hz)	Measured P_{out} (dBm)	Die Area (mm^2)	Ref.
0.25µm CMOS	63	1.8	118.8	-85	1	-160.2	-4	0.315	ISSCC04 [5]
0.25µm SiGe BiCMOS	37	4	84	-105	2	-171.1	-14	0.28	ISSCC04 [6]
0.25µm SiGe BiCMOS	60	-3	73.8	-87	1	-163.9	-17	0.28	ISSCC03 [7]
0.25µm SiGe BiCMOS	76	-4	128	-91	1	-167.5	-7	0.28	ISSCC03 [7]
90nm CMOS	100	1	120	-110	10	-169.2	-65	-	ISSCC04 [8]
0.18µm CMOS	52.5	-	41	-86	1	-164.3	-8	0.8	RFIC04 [9]
0.13µm CMOS	114	1.2	8.4	-107.6	10	-179.5	> -22.5	0.2	This Work

$$* \; F.O.M. = -10log[(\frac{f_o}{f_m})^2(\frac{1}{L(m)\cdot P})]$$

Figure 21.8.6: Summary of measured performance and comparison with recently reported Si-based MMW VCOs.

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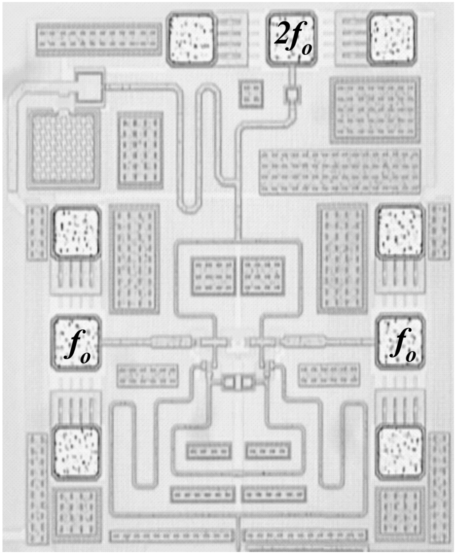

Figure 21.8.7: Chip micrograph of the D-band CMOS VCO (0.42x.48mm^2).

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