

Objective

To find a full-time computer engineering R&D position. Specific interests include:

- Models of Computation and Computer System Architectures for Emerging Nanotechnologies
- Reliability-Aware and Power-Aware System Design
- Computer Architecture, Embedded Systems, Compilers, Design Tools

Education

- **The University of Texas at Austin** Austin, TX
PhD candidate in Computer Engineering Jan. 2003 - Dec. 2009
 - Advisor Prof. Gustavo de Veciana (co-advisor Prof. Margarida F. Jacome)
 - PhD thesis topic: “Exploring Scaling Limits and Computational Paradigms for Next Generation Embedded Systems”.
- **Moscow Institute of Physics and Technology** Moscow, Russia
MS/BS in Electrical Engineering 1993-1999
 - MS thesis project: “Numerical simulation of integrated logic elements and memory cells based on MOS and bipolar transistor structures”.

Industry Experience

- **Magma Design Automation** Austin, TX
Internship, Circuit Simulation Group June 2008 - November 2008
 - Research and development for circuit level simulator ‘finesim’ (C++, linux).
 - Projects: RC reduction.
- **Sky Links Systems** Moscow, Russia
Programmer March 2002 - December 2002
 - Development of web applications on platform Windows 2000 Server, IIS5, MS Access 2000 (SSI, ASP + Visual Basic server ActiveX, SQL, XML). Development of GUI applications on Windows platform (Visual Basic, Visual C++, COM, GUI ActiveX, XML).
 - Projects: internet web frontend for GPRS/GSM logistics system, tools for this system.
- **3WStyle** Moscow, Russia
Technical Manager August 2001 - February 2002
 - Development of web applications on platform Windows 2000 Server, IIS5, MS SQL Server (SSI, ASP + Visual Basic/Visual C++ server ActiveX, HTML, SQL). Basic administration of Windows 2000 Server (web /IIS5/, DNS, MS SQL Server 2000, MS Source Safe Server, Windows 2000 Domain Server), Linux/FreeBSD servers (router, firewall /ipchains/, mail /sendmail, majordomo/, web /apache, perl/shell CGI scripts, php/, ftp) and technical administration of Internet domain names.
 - Projects: intranet web bank system, web based system for projects & tasks management.

- **Galaktika Corp** Moscow, Russia
Programmer: Search and Analytical Systems Department (InfoTame) *June 1999 - July 2001*
 – Research and development for statistical content analysis of text databases (Windows NT platform, Visual C++).
 – Projects: statistical analysis modules for Galaktika-ZOOM/ITee software package.
- **NICOTECH** Moscow, Russia
Programmer (part time) *January 1998 - May 1998*
 – Development of Windows GUI for remote AS/400 information system (MS Visual Basic, GUI ActiveX).

Academic Research Experience

- **The University of Texas at Austin** Austin, TX
Research Assistant *September 2004 - present*
 – Working with Prof. Margarida F. Jacome and Prof. Gustavo de Veciana on models of computation and platforms for emerging nanotechnology.
 – Supported by GSRC, NSF
- **The University of Texas at Austin** Austin, TX
MCD Fellowship *January 2003 - August 2004*
 – (the same as above).
- **Moscow Institute of Physics and Technology** Moscow, Russia
Student *September 1996 - May 1999*
 – Working with Prof. A. N. Bubennikov on device-circuit simulator of semiconductor structures and logical elements.

Publications

1. Efficient estimation & sensitivity analysis of SRAM yield. A. Zykov, G. de Veciana. In preparation, 2009.
2. Revisiting methods for solving linear equations associated with mesh circuits. A. Zykov, G. de Veciana. In preparation, 2009.
3. Using Randomly Assembled Networks for Computation. Andrey V. Zykov, Gustavo de Veciana. *Third International Conference on Nano-Networks (Nano-Net 2008)*, 2008.
4. Exploring Density-Reliability Tradeoffs on Nanoscale Substrates: When do smaller less reliable devices make sense? Andrey V. Zykov, Gustavo de Veciana. *The 23rd IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems (DFT'08)*, 2008.
5. Perturbation-Based Computing for Next-Generation Embedded IT Targeted at Emerging Nanoelectronics. Andrey V. Zykov, Margarida F. Jacome, Gustavo de Veciana. Submitted for Publication, 2009.
6. High Performance Computing on Fault-Prone Nanotechnologies: Novel Microarchitecture Techniques Exploiting Reliability-Delay Trade-offs. Andrey V. Zykov, Elias Mizan, Margarida F. Jacome, Gustavo de Veciana, Ajay Subramanian. In *Proc. IEEE/ACM Design Automation Conference (DAC)*, 2005.

7. High Performance Computing on Fault-Prone Nanotechnologies: Novel Microarchitecture Techniques Exploiting Reliability-Delay Trade-offs. Andrey V. Zykov, Elias Mizan, Margarida F. Jacome, Gustavo de Veciana, Ajay Subramanian. Technical Report CERC-TR-MJ-0502, 2005.
8. On Nanotechnology's Fundamental Scaling Limits: A Study On The Impact Of Robustness To Delay Uncertainty On A Design's Performance And Area. Stephen Bijansky, Andrey Zykov, and Margarida Jacome. Technical Report CERC-TR-MJ-0503, 2005.

Relevant Coursework (overall GPA 3.9):

- Simulation Methods in CAD/VLSI (*taught by Anirudh Devgan, Fall'07*)
- Computer Vision Systems (*taught by J.K. Aggarwal, Spring'06*)
- Digital Signal Processing (*taught by Alan C. Bovik, Fall'05*)
- Advanced Compilers (*taught by Kathryn S. McKinley, Fall'04*)
 - Implemented profiling driven loop unrolling/flattening in Java compiler (Jikes RVM)
- Microarchitecture (*taught by Yale N. Patt, Spring'04*)
 - Implemented in structural Verilog processor (pipeline, icache, dcache, interrupts, exceptions) for given subset of x86 ISA
- Optimization in Engineering Systems (*taught by Ross Baldick, Spring'04*)
- Probability and Stochastic Processes (*taught by Gustavo de Veciana, Fall'03*)
- Compilers (*taught by Daniel P. Miranker, Fall'03*)
- VLSI (*taught by Raghuram S. Tupuri, Spring'03*)
 - Implemented in structural Verilog fast combinatorial 32bit floating point multiplier (using Wallace tree integer multiplier)
- Dependable Computing (*taught by Nur A. Touba, Spring'03*)
 - Implemented in structural Verilog 3bit redundant ALU with fault indicating output (tested by fault injection at internal nodes)
- Computer Architecture (*taught by Yale N. Patt, Spring'03*)
 - Wrote in C a simulator and assembler for a 16bit RISC microprocessor (the LC3b - in-order pipeline, exceptions, interrupts, virtual memory)

Miscellaneous

Technical Skills: MATLAB, C/C++, Verilog, PSPICE, Java, Fortran, Linux OS (perl/shell/php scripting), Windows NT/2000/XP OS (Visual Studio, COM, ASP), DHTML, SQL

Membership: IEEE, ACM, Sigma Xi

Hobbies: swimming, hiking

Current Visa Status: F-1

References: upon request