Motivation

- The following common source configuration needs to have its gate biased at 500mV

\[ \begin{align*}
V_G &= 1V \\
R_1 &= 1kΩ \\
R_2 &= \frac{V_{OUT}}{2} = 500mV \\
V_T &= 300mV \\
V_B &= \frac{V_{OUT}}{2} = 500mV
\end{align*} \]

Solution #1: Voltage bias

Q: what happens if \( V_T \) is 50mV smaller? (Process, Temp. variation)

A:

Equations:

1. \( I_{out} = \frac{9.5V}{1000Ω} = 500µA \)
2. \( I_{out1} = \frac{500µA}{2} = \frac{(500mV - 300mV)^2}{200mV} \)
3. \( I_{out2} = \frac{(250mV)^2}{(200mV)^2} \)
4. \( I_{out2} = 500µA \times \frac{0.0625}{0.04} = 500µA \times 1.5625 = 781µA \)

\[ V_{OUT} = 1V - 781mA \times 1kΩ = 219mV \]

because \( V_{OUT} < V_G - V_T \)

\( \rightarrow \) M1 is no more working in saturation.

BAD BRAIN TECHNIQUE

Solution #2: Current bias

Q: what happens if \( V_T \) is 50mV smaller?

A: assuming \( r_{01}, r_{02} = \infty \), \( M1, M2 \) are identical and \( I_b = 500µA \),
the output voltage will remain unchanged and the circuit will keep working.

GOOD BRAIN TECHNIQUE

\( \triangle \) Cross transistors are always biased using currents! Do never use absolute voltages, even when you are "playing" with simulator.
Example of an easy way to generate a reference current:

Finding $R$:
- $I_{in}$ is known
- $B = \frac{I_{in}}{V}$ is also known
- $V_{gs} = \frac{\sqrt{2}I_{in}}{B} + V_T$
- $V_{dd} - V_{gs} = V_{dd} - V_T - \sqrt{\frac{2I_{in}}{B}}$

The resistor is usually off-chip so that one can tweak it to change the bias current and supply voltage independency are required. A bandgap-based reference generator is used.

**Principle**

$$I_1 = \frac{1}{N} I_2$$

$$\left\{ \begin{array}{l}
I_1 = \frac{W_1}{L_1} (V_{gs1} - V_T)^2 (1 + M_1 V_{gs1}) \\
I_2 = \frac{W_2}{L_2} (V_{gs1} - V_T)^2 (1 + M_2 V_{gs2}) \\
\frac{I_1}{I_2} = \frac{W_1}{W_2} \frac{1 + \lambda_1 V_{gs1}}{1 + \lambda_2 V_{gs2}}
\end{array} \right.$$

Note that $M_1$ is always in saturation because $V_{gs1} = V_{gs1} > V_{gs2} - V_T$.

- If the output impedance is $\infty$, i.e., $\lambda_2 = \lambda_2 = 0$ then the current ratio is $N = \frac{W_2}{W_1}$.

- Big $N$'s ($N=10$ to $20$) are used to reduce the bias current $I_1$ assuming the operating current $I_2$ is fixed.

- The NMOS mirror is called current sink. The PMOS mirror is called current source.
Two real transistors are never identical.

\[
\begin{align*}
\sigma_{\Delta V_T} &= \frac{A_{VT}}{\sqrt{VWL}} \\
\frac{\sigma_{\Delta I}}{I_{DS}} &= \frac{A_{\beta}}{\sqrt{VWL}}
\end{align*}
\]

- \( A_{VT} \) and \( A_{\beta} \) are two empirically measured constants.
- \( \sigma_{\Delta V_T} \) and \( \sigma_{\Delta I} \) are the standard deviations of variables that are assumed to have a Gaussian distribution.
- \( \Delta V_T \) and \( \Delta \beta \) are random variables like noise therefore they add in rms way.
- The correlation between \( V_T \) and \( \beta \) is very low therefore their effect adds in rms way as well.

- Note that usually \( \sigma_{\Delta V_T} \) and \( \sigma_{\Delta I} \) are given as the \( \sigma \) between two devices. The \( \sigma \) of a single device from its nominal value is \( \sqrt{2} \) smaller:

\[
\bar{V}_{\Delta V_T}^2 = \sigma_{\Delta V_T, in}^2 + \sigma_{\Delta V_T, abs}^2
\]

\[
= 2 \sigma_{\Delta V_T, abs}^2 \quad \text{[if devices have the same size]}
\]

\[
\sigma_{\Delta V_T, abs} = \frac{\sigma_{\Delta V_T}}{2}
\]

- The way two transistors are laid out can affect their matching factors. The more symmetric they are the better they match.

\[
\sigma_{\Delta V_T} \approx 2.5 \text{mV}
\]

For a deep sub-micron technology.
Due to transistor mismatch, the current will never be the same in a mirror, even if \( V_{DS1} = V_{DS2} = V_{AS1} \).

Current mismatch calculation:

\[
\frac{\Delta I^2}{I_2} = \left( \frac{V_{GS1} + V_{GS2}}{2} \right) \frac{g_{m2}}{g_{m1}} = \frac{g_{m2}}{g_{m1}} \cdot \left( 2 \left( \frac{V_{GS1} - V_T}{2} \right)^2 + \left( \frac{V_{GS2} - V_T}{2} \right)^2 \right)
\]

\[
= \frac{g_{m2}}{g_{m1}} \cdot \left[ \frac{1}{2} \left( \frac{V_{GS1} - V_T}{2} \right)^2 + \left( \frac{V_{GS2} - V_T}{2} \right)^2 \right]
\]

\[
= \frac{I \chi'N}{2 L_1} \left[ \left( 1 + \frac{1}{N} \right) \left( \frac{A_{\Delta V_T}^2}{2} + \frac{A_{\Delta V_T}^2}{2} \right) \right]
\]

\[
= \frac{I \chi'N}{L_1^2} \left[ \left( 1 + \frac{1}{N} \right) \left( A_{\Delta V_T}^2 + V_{GS1}^2 - V_T^2 \right) \right]
\]

\[
= \left( \frac{\Delta I^2}{I_2} \right)^2 = \frac{\chi'N}{L_1^2} \left( 1 + \frac{1}{N} \right) \left[ A_{\Delta V_T}^2 + A_{\Delta V_T}^2 \left( V_{GS1} - V_T \right)^2 \right]
\]

- Matching improves \( L_1 \)
- Matching gets worse when \( \sqrt{N} \)

The second term in the brackets is usually negligible for normal \( V_{GS} - V_T \), however it can contribute if \( V_{GS} - V_T \) is big.

If more mirrors are connected to the chain, the current errors will sum in an RMS way.

\( V_{GS} = V_{GS1} \)
\( L_2 = L_1 \)
\( W_2 = NW_1 \)
Mismatch due to voltage asymmetry

As we have seen before, if the transistor $\lambda_1, \lambda_2 \neq 0$ and $V_{gs1} \neq V_{ds2}$, we there is a deterministic mismatch of the mirror currents. → maximize $V_o$

\[
\frac{I_1}{I_2} = \frac{1 + \lambda_1 V_{gs1}}{1 + \lambda_2 V_{ds2}}
\]

Cascode Current Mirrors

In the last class, we showed that the cascode structure can boost the transistor impedance.

**Cascode Mirror #1**

- $\lambda$ is reduced by a factor $\frac{W_m}{W_2}$

- $V_{out_{min}}$ - large minimum $V_{out}$ to keep $M_2, M_2C$ in saturation

$\Rightarrow V_{out_{min}} = V_{gs1} + V_{gs2} - V_{T2} = V_{DSat1} + V_{DSat2} + V_T$

**Cascode Mirror #2**

- $V_b$ can be selected such that $V_{out_{min}} = V_{DSat2} + V_{DSat2C} \Rightarrow V_{out_{min}}$ is small

- High output impedance

\[ \Rightarrow I_2 \text{ is insensitive to variations of } V_{out} \]

- Not precise because $\lambda_1$ is still high

- Needs an additional bias current
Cascode Mirror #3

+ : both sides of the mirror are high impedance
+ : \( V_{out, min} = V_{sat2} + V_{sat2c} \) can be obtained
- : needs an additional bias current

Cascode Mirror #4

+ : both sides are high impedance
+ : \( V_{out, min} \)
+ : no additional bias current needed
- : \( V_b \) does not always track process temp variations
  \( V_{out, min} \) is not always optimum