DACs 1

Fig. 12.1 Resistor-string 3-bit D/A converter with a transmission-gate, tree-like decoder.

\[ B_{in} = b_12^{-1} + b_22^0 + b_32^1 \]

Fig. 12.12 Binary-array charge-redistribution D/A converter.

Fig. 12.13 Binary-weighted current-mode D/A converter.
**Fig. 13.16** A 3-bit flash A/D converter.

**Fig. 12.10** 4-bit R-2R based D/A converter.
Comparator

\[ \text{Fig. 7.20} \quad \text{A simplified schematic of the comparator described in [Razavi, 1992].} \]

\[ \text{Fig. 7.13} \quad \text{A typical architecture for a high-speed comparator.} \]
AOCs 2

Fig. 13.7 A 5-bit unipolar charge-redistribution A/D converter.

Fig. 13.4 Flow graph for the successive-approximation approach.
ADCs 3

Fig. 13.13 Flow graph for the algorithmic approach.

Fig. 13.31 A pipelined A/D converter.

Fig. 13.32 A 1-bit digital approximator (DAPRX).

Fig. 13.14 Algorithmic converter.