2. CMOS Fabrication, Layout, Design Rules

- Last module:
  - Introduction to the course
  - How a transistor works
  - CMOS transistors

This module:
- CMOS Fabrication
- Design Rules

CMOS Fabrication
- CMOS transistors are fabricated on silicon wafers
- Lithography process has been the mainstream chip manufacturing process
  - Similar to printing press
  - See Chris Mack's page for a nice litho tutorial
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

Inverter Cross-section
- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors

Well and Substrate Taps
- Substrate must be tied to GND, n-well to VDD
- Metal to lightly-doped semiconductor forms poor connection called Shottky Diode
- Use heavily doped well and substrate contacts / taps

Inverter Mask Set
- Transistors and wires are defined by masks
- Cross-section taken along dashed line

Detailed Mask Views
- Six masks
  - n-well
  - Polysilicon
  - n+ diffusion
  - p+ diffusion
  - Contact
  - Metal
Fabrication Steps

- Start with blank wafer
- Build inverter from the bottom up
- First step will be to form the n-well
  - Cover wafer with protective layer of SiO₂ (oxide)
  - Remove layer where n-well should be built
  - Implant or diffuse n dopants into exposed wafer
  - Strip off SiO₂

Oxidation

- Grow SiO₂ on top of Si wafer
  - 900 – 1200 °C with H₂O or O₂ in oxidation furnace

Photoresist

- Spin on photoresist
  - Photoresist is a light-sensitive organic polymer
  - Softens where exposed to light

Lithography

- Expose photoresist through n-well mask
- Strip off exposed photoresist

Etch

- Etch oxide with hydrofluoric acid (HF)
  - Seeps through skin and eats bone; nasty stuff!!
- Only attacks oxide where resist has been exposed

Strip Photoresist

- Strip off remaining photoresist
  - Use mixture of acids called piranah etch
- Necessary so resist doesn’t melt in next step
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**n-Well**
- n-well formed with diffusion or ion implant
- Diffusion
  - Place wafer in furnace with arsenic gas
  - Heat until As atoms diffuse into exposed Si
- Ion Implantation
  - Blast wafer with beam of As ions
  - Ions blocked by SiO₂, only enter exposed Si

**Strip Oxide**
- Strip off the remaining oxide using HF
- Back to bare wafer with n-well
- Subsequent steps involve similar series of steps

**Polysilicon**
- Deposit very thin layer of gate oxide
  - < 20 Å (6-7 atomic layers)
- Chemical Vapor Deposition (CVD) of Si layer
  - Place wafer in furnace with Silane gas (SiH₄)
  - Forms many small crystals called polysilicon
  - Heavily doped to be good conductor

**Polysilicon Patterning**
- Use same lithography process to pattern polysilicon

**Self-Aligned Process**
- Use oxide and masking to expose where n+ dopants should be diffused or implanted
- N-diffusion forms nMOS source, drain, and n-well contact

**N-diffusion**
- Pattern oxide and form n+ regions
- *Self-aligned process* - gate blocks diffusion
- Polysilicon is better than metal for self-aligned gates because it doesn’t melt during later processing
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N-diffusion, Cont’d
- Historically dopants were diffused
- Usually ion implantation today
- But regions are still called diffusion

P-Diffusion
- Similar set of steps form p+ diffusion regions for pMOS source and drain and substrate contact

Contacts
- Now we need to wire together the devices
- Cover chip with thick field oxide
- Etch oxide where contact cuts are needed

Metallization
- Sputter on aluminum over whole wafer
- Pattern to remove excess metal, leaving wires

Layout
- Describes actual layers and geometry on the silicon substrate to implement a function
- Need to define transistors, interconnection
  - Transistor widths (for performance)
  - Spacing, interconnect widths, to reduce defects, satisfy power requirements
  - Contacts (between poly or active and metal), and vias (between metal layers)
  - Wells and their contacts (to power or ground)
- Layout of lower-level cells constrained by higher-level requirements: “floorplanning”
  - “design iteration”
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Layout, Cont’d

• Chips are specified with set of masks
• Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
• Feature size $f =$ distance between source and drain
  – Set by minimum width of polysilicon
• Feature size improves 30% every 3 years or so
• Normalize for feature size when describing design rules
• Express rules in terms of $\lambda = f/2$
  – E.g. $\lambda = 0.3 \mu m$ in 0.6 $\mu m$ process

CMOS Inverter Layout

Note: the N- and P-wells are not shown here

Another CMOS Inverter Layout

CMOS Inverter with Wider Transistors

Buffer with Two Inverters

Buffer with Stacked Inverters
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Efficient Buffer with Stacked Inverters

“Stick” Diagram for NAND Gate
• Identifies actual layers, can be annotated with transistor sizes

Simplified Layout of NAND Gate

Simplified Design Rules
• Conservative rules to get you started

Inverter Layout
• Transistor dimensions specified as Width / Length
  – Minimum size $4\lambda / 2\lambda$, sometimes called 1 unit
  – In $f = 0.6 \mu m$ process, this is 1.2 $\mu m$ wide, 0.6 $\mu m$ long

The MOSIS Scalable CMOS Rules
• $\lambda$-based rules
• Designs using these rules are fabricated by a variety of companies
• Multiple designs are put on a single die
  – Each chip wired to a particular design
• Support for submicron digital CMOS, analog (buried poly layer for capacitor), micromachines, etc.
Advanced Metallization

Cu and the Damascene Process

Layers of Damascene Copper (Intel)

Copper Damascene Interconnects (Intel)

Advanced Metallization

Silicon on Insulator (SOI)

Thin layer of Si (a few microns) deposited on an insulator

Devices separated from one another by anisotropic etching