Introduction to High-Level Synthesis with Vivado HLS

Vivado HLS 2013.3 Version

Objectives

After completing this module, you will be able to:

- Describe the high level synthesis flow
- Understand the control and datapath extraction
- Describe scheduling and binding phases of the HLS flow
- List the priorities of directives set by Vivado HLS
- List comprehensive language support in Vivado HLS
- Identify steps involved in validation and verification flows
Outline

- Introduction to High-Level Synthesis
- High-Level Synthesis with Vivado HLS
- Language Support
- Validation Flow
- Summary

High-Level Synthesis: HLS

- High-Level Synthesis
  - Creates an RTL implementation from C level source code
  - Extracts control and dataflow from the source code
  - Implements the design based on defaults and user applied directives

- Many implementation are possible from the same source description
  - Smaller designs, faster designs, optimal designs
  - Enables design exploration
Design Exploration with Directives

One body of code:
Many hardware outcomes

The same hardware is used for each iteration of the loop:
• Small area
• Long latency
• Low throughput

Before we get into details, let’s look under the hood ....

Different hardware is used for each iteration of the loop:
• Higher area
• Short latency
• Best throughput

Different iterations are executed concurrently:
• Higher area
• Short latency
• Best throughput

Introduction to High-Level Synthesis

How is hardware extracted from C code?
  – Control and datapath can be extracted from C code at the top level
  – The same principles used in the example can be applied to sub-functions
    • At some point in the top-level control flow, control is passed to a sub-function
    • Sub-function may be implemented to execute concurrently with the top-level and or other sub-functions

How is this control and dataflow turned into a hardware design?
  – Vivado HLS maps this to hardware through scheduling and binding processes

How is my design created?
  – How functions, loops, arrays and IO ports are mapped?
HLS: Control Extraction

```
void fir (data_t *y, coef_t c[4], data_t x) {
    static data_t shift_reg[4];
    acc_t acc;
    int i;
    acc=0;
    loop: for (i=3;i>=0;i--) {
        if (i==0) {
            acc+=x*c[0];
            shift_reg[0]=x;
        } else {
            shift_reg[i]=shift_reg[i-1];
            acc+=shift_reg[i]*c[i];
        }
    }
    *y=acc;
}
```

From any C code example...
The loops in the C code correlated to states of behavior
This behavior is extracted into a hardware state machine

HLS: Control & Datapath Extraction

```
void fir (data_t *y, coef_t c[4], data_t x) {
    static data_t shift_reg[4];
    acc_t acc;
    int i;
    acc=0;
    loop: for (i=3;i>=0;i--) {
        if (i==0) {
            acc+=x*c[0];
            shift_reg[0]=x;
        } else {
            shift_reg[i]=shift_reg[i-1];
            acc+=shift_reg[i]*c[i];
        }
    }
    *y=acc;
}
```

From any C code example...
Operations are extracted...
The control is known
A unified control dataflow behavior is created.
High-Level Synthesis: Scheduling & Binding

- **Scheduling & Binding**
  - Scheduling and Binding are at the heart of HLS
  - Scheduling determines in which clock cycle an operation will occur
    - Takes into account the control, dataflow and user directives
    - The allocation of resources can be constrained
  - Binding determines which library cell is used for each operation
    - Takes into account component delays, user directives

![Diagram of Scheduling and Binding](image)

**Scheduling**

- The operations in the control flow graph are mapped into clock cycles

```
void foo (
    ...
    t1 = a * b;
    t2 = c + t1;
    t3 = d * t2;
    out = t3 - e;
}
```

- The technology and user constraints impact the schedule
  - A faster technology (or slower clock) may allow more operations to occur in the same clock cycle

- The code also impacts the schedule
  - Code implications and data dependencies must be obeyed
# Binding

- Binding is where operations are mapped to cores from the hardware library
  - Operators map to cores

- **Binding Decision: to share**
  - Given this schedule:
    - Binding must use 2 multipliers, since both are in the same cycle
    - It can decide to use an adder and subtractor or share one addsub

- **Binding Decision: or not to share**
  - Given this schedule:
    - Binding may decide to share the multipliers (each is used in a different cycle)
    - Or it may decide the cost of sharing (muxing) would impact timing and it may decide not to share them
    - It may make this same decision in the first example above too

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Understanding Vivado HLS Synthesis

- **HLS**
  - Vivado HLS determines in which cycle operations should occur (scheduling)
  - Determines which hardware units to use for each operation (binding)
  - It performs HLS by:
    - Obeying built-in defaults
    - Obeying user directives & constraints to override defaults
    - Calculating delays and area using the specified technology/device

- **Understand the priority of directives**
  1. Meet Performance (clock & throughput)
     - Vivado HLS will allow a local clock path to fail if this is required to meet throughput
     - Often possible the timing can be met after logic synthesis
  2. Then minimize latency
  3. Then minimize area

The Key Attributes of C code

- **Functions**: All code is made up of functions which represent the design hierarchy; the same in hardware
- **Top Level IO**: The arguments of the top-level function determine the hardware RTL interface ports
- **Types**: All variables are of a defined type. The type can influence the area and performance
- **Loops**: Functions typically contain loops. How these are handled can have a major impact on area and performance
- **Arrays**: Arrays are used often in C code. They can influence the device IO and become performance bottlenecks
- **Operators**: Operators in the C code may require sharing to control area or specific hardware implementations to meet performance

Let’s examine the default synthesis behavior of these …
Functions & RTL Hierarchy

Each function is translated into an RTL block
- Verilog module, VHDL entity
- Source Code
  ```c
  void A() { ..body A.. }
  void B() { ..body B.. }
  void C() { B(); }
  void D() { B(); }
  void foo_top() {
    A(…);
    C(…);
    D(…)
  }
  ```
- By default, each function is implemented using a common instance
- Functions may be inlined to dissolve their hierarchy
  - Small functions may be automatically inlined

RTL hierarchy
- foo_top
  - A
  - B
  - C
  - D

Each function/block can be shared like any other component (add, sub, etc) provided
it's not in use at the same time

Types = Operator Bit-sizes

Code
```c
void fir (data_t *y, coef_t c[4], data_t x) {
  static data_t shift_reg[4];
  acc_t acc;
  int i;
  acc=0;
  loop: for (i=3;i>=0;i--)
    if (i==0)
      acc+=x*c[0];
      shift_reg[0]=x;
    else
      shift_reg[i]=shift_reg[i-1];
      acc+=shift_reg[i]*c[i];
  *y=acc;
}
```
Loops

➤ By default, loops are rolled
  - Each C loop iteration ➔ Implemented in the same state
  - Each C loop iteration ➔ Implemented with same resources

Loops require labels if they are to be referenced by Tcl directives
(GUI will auto-add labels)

➤ Loops can be unrolled if their indices are statically determinable at elaboration time
  - Not when the number of iterations is variable
  - Unrolled loops result in more elements to schedule but greater operator mobility
  - Let’s look at an example ….

```c
void foo_top (...) {
  ...
  Add: for (i=3;i>=0;i--) {
    b = a[i] + b;
  ...
}
```

Data Dependencies: Good

➤ Example of good mobility
  - The read on data port X can occur anywhere from the start to iteration 4
    - The only constraint on RDx is that it occur before the final multiplication
  - Vivado HLS has a lot of freedom with this operation
    - It waits until the read is required, saving a register
    - There are no advantages to reading any earlier (unless you want it registered)
    - Input reads can be optionally registered
  - The final multiplication is very constrained…
Data Dependencies: Bad

Example of bad mobility
- The final multiplication must occur before the read and final addition
  - It could occur in the same cycle if timing allows
- Loops are rolled by default
  - Each iteration cannot start till the previous iteration completes
  - The final multiplication (in iteration 4) must wait for earlier iterations to complete
- The structure of the code is forcing a particular schedule
  - There is little mobility for most operations
- Optimizations allow loops to be unrolled giving greater freedom

Schedule after Loop Optimization

With the loop unrolled (completely)
- The dependency on loop iterations is gone
- Operations can now occur in parallel
  - If data dependencies allow
  - If operator timing allows
- Design finished faster but uses more operators
  - 2 multipliers & 2 Adders

Schedule Summary
- All the logic associated with the loop counters and index checking are now gone
- Two multiplications can occur at the same time
  - All 4 could, but it’s limited by the number of input reads (2) on coefficient port C
- Why 2 reads on port C?
  - The default behavior for arrays now limits the schedule...
**Arrays in HLS**

- An array in C code is implemented by a memory in the RTL
  - By default, arrays are implemented as RAMs, optionally a FIFO
  - The array can be targeted to any memory resource in the library
    - The ports (Address, CE active high, etc.) and sequential operation (clocks from address to data out) are defined by the library model
    - All RAMs are listed in the Vivado HLS Library Guide
- Arrays can be merged with other arrays and reconfigured
  - To implement them in the same memory or one of different widths & sizes
- Arrays can be partitioned into individual elements
  - Implemented as smaller RAMs or registers

```c
void foo_top(int x, ...) {
    int A[N];
    L1: for (i = 0; i < N; i++)
}
```

**Top-Level IO Ports**

- Top-level function arguments
  - All top-level function arguments have a default hardware port type
- When the array is an argument of the top-level function
  - The array/RAM is "off-chip"
  - The type of memory resource determines the top-level IO ports
  - Arrays on the interface can be mapped & partitioned
    - E.g. partitioned into separate ports for each element in the array

```c
void foo_top(int A[3*N], int x) {
    L1: for (i = 0; i < N; i++)
}
```

- Default RAM resource
  - Dual port RAM if performance can be improved otherwise Single Port RAM
Schedule after an Array Optimization

- With the existing code & defaults
  - Port C is a dual port RAM
  - Allows 2 reads per clock cycles
    - IO behavior impacts performance

Note: It could have performed 2 reads in the original rolled design but there was no advantage since the rolled loop forced a single read per cycle.

- With the C port partitioned into (4) separate ports
  - All reads and mults can occur in one cycle
  - If the timing allows
    - The additions can also occur in the same cycle
    - The write can be performed in the same cycles
    - Optionally the port reads and writes could be registered

Operators

- Operator sizes are defined by the type
  - The variable type defines the size of the operator

- Vivado HLS will try to minimize the number of operators
  - By default Vivado HLS will seek to minimize area after constraints are satisfied

- User can set specific limits & targets for the resources used
  - Allocation can be controlled
    - An upper limit can be set on the number of operators or cores allocated for the design: This can be used to force sharing
    - e.g. limit the number of multipliers to 1 will force Vivado HLS to share
  - Resources can be specified
    - The cores used to implement each operator can be specified
    - e.g. Implement each multiplier using a 2 stage pipelined core (hardware)
Outline

➤ Introduction to High-Level Synthesis
➤ High-Level Synthesis with Vivado HLS
➤ Language Support
➤ Validation Flow
➤ Summary

Comprehensive C Support

➤ A Complete C Validation & Verification Environment
  – Vivado HLS supports complete bit-accurate validation of the C model
  – Vivado HLS provides a productive C-RTL co-simulation verification solution

➤ Vivado HLS supports C, C++ and SystemC
  – Functions can be written in any version of C
  – Wide support for coding constructs in all three variants of C

➤ Modeling with bit-accuracy
  – Supports arbitrary precision types for all input languages
  – Allowing the exact bit-widths to be modeled and synthesized

➤ Floating point support
  – Support for the use of float and double in the code

➤ Support for OpenCV functions
  – Enable migration of OpenCV designs into Xilinx FPGA
  – Libraries target real-time full HD video processing
C, C++ and SystemC Support

- The vast majority of C, C++ and SystemC is supported
  - Provided it is statically defined at compile time
  - If it's not defined until run time, it won't be synthesizable

- Any of the three variants of C can be used
  - If C is used, Vivado HLS expects the file extensions to be .c
  - For C++ and SystemC it expects file extensions .cpp

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There are two steps to verifying the design

- Pre-synthesis: C **Validation**
  - Validate the algorithm is correct
- Post-synthesis: RTL **Verification**
  - Verify the RTL is correct

**C validation**

- A HUGE reason users want to use HLS
  - Fast, free verification
- Validate the algorithm is correct **before** synthesis
  - Follow the test bench tips given over

**RTL Verification**

- Vivado HLS can co-simulate the RTL with the original test bench

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**C Function Test Bench**

- The test bench is the level above the function
  - The main() function is **above** the function to be synthesized

**Good Practices**

- The test bench should compare the results with golden data
  - Automatically confirms any changes to the C are validated and verifies the RTL is correct
- The test bench should return a 0 if the self-checking is correct
  - Anything but a 0 (zero) will cause RTL verification to issue a FAIL message
- Function main() should expect an integer return (non-void)

```c
int main() {
    int ret;
    ret = system("diff --brief -w output.dat output.golden.dat");
    if (ret != 0) {
        print("Test failed \n");
        return 1;
    } else {
        print("Test passed in\n");
    }
    return ret;
}
```
Determine or Create the top-level function

- Determine the top-level function for synthesis
- If there are Multiple functions, they must be merged
  - There can only be 1 top-level function for synthesis

> Given a case where functions func_A and func_B are to be implemented in FPGA

> Re-partition the design to create a new single top-level function inside main()

Recommendation is to separate test bench and design files

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Summary

- **In HLS**
  - C becomes RTL
  - Operations in the code map to hardware resources
  - Understand how constructs such as functions, loops and arrays are synthesized

- **HLS design involves**
  - Synthesize the initial design
  - Analyze to see what limits the performance
    - User directives to change the default behaviors
    - Remove bottlenecks
  - Analyze to see what limits the area
    - The types used define the size of operators
    - This can have an impact on what operations can fit in a clock cycle

- **Use directives to shape the initial design to meet performance**
  - Increase parallelism to improve performance
  - Refine bit sizes and sharing to reduce area
Using Vivado HLS

Vivado HLS 2013.3 Version

Objectives

After completing this module, you will be able to:

- List various OS under which Vivado HLS is supported
- Describe how projects are created and maintained in Vivado HLS
- State various steps involved in using Vivado HLS project creation wizard
- Distinguish between the role of top-level module in testbench and design to be synthesized
- List various verifications which can be done in Vivado HLS
- List Vivado HLS project directory structure
Outline

» Invoking Vivado HLS
» Project Creation using Vivado HLS
» Synthesis to IPXACT Flow
» Design Analysis
» Other Ways to use Vivado HLS
» Summary

Invoke Vivado HLS from Windows Menu

The first step is to open or create a project.
Outline

- Invoking Vivado HLS
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Vivado HLS Projects and Solutions

- **Vivado HLS is project based**
  - A project specifies the source code which will be synthesized
  - Each project is based on one set of source code
  - Each project has a user specified name
- **A project can contain multiple solutions**
  - Solutions are different implementations of the same code
  - Auto-named solution1, solution2, etc.
  - Supports user specified names
  - Solutions can have different clock frequencies, target technologies, synthesis directives
- **Projects and solutions are stored in a hierarchical directory structure**
  - Top-level is the project directory
  - The disk directory structure is identical to the structure shown in the GUI project explorer (except for source code location)

Vivado HLS Step 1: Create or Open a project

- **Start a new project**
  - The GUI will start the project wizard to guide you through all the steps
- **Open an existing project**
  - All results, reports and directives are automatically saved/remembered
  - Use “Recent Project” menu for quick access
Project Wizard

The Project Wizard guides users through the steps of opening a new project.

- Define project and directory
- Add design source files
- Specify test bench files
- Specify clock and select part

Step-by-step guide …

Define Project & Directory

- Define the project name
  - Note, here the project is given the extension .prj
  - A useful way of seeing it’s a project (and not just another directory) when browsing

- Browse to the location of the project
  - In this example, project directory “dct.prj” will be created inside directory “lab1”
Add Design Source Files

- **Add Design Source Files**
  - This allows Vivado HLS to determine the top-level design for synthesis, from the test bench & associated files
  - Not required for SystemC designs

- **Add Files**
  - Select the source code file(s)
  - The CTRL and SHIFT keys can be used to add multiple files
  - No need to include headers (.h) if they reside in the same directory

- **Select File and Edit CFLAGS**
  - If required, specify C compile arguments using the “Edit CFLAGS…”
  - Define macros: `#DVERSION1`
  - Location of any (header) files not in the same directory as the source: `-I../include`

There is no need to add the location of standard Vivado HLS or SystemC header files or header files located in the same project location.

Specify Test Bench Files

- **Use “Add Files” to include the test bench**
  - Vivado HLS will re-use these to verify the RTL using co-simulation

- **And all files referenced by the test bench**
  - The RTL simulation will be executed in a different directory (Ensures the original results are not over-written)
  - Vivado HLS needs to also copy any files accessed by the test bench
  - Input data and output results (*.dat) are shown in this example

- **Add Folders**
  - If the test bench uses relative paths like “sub_directory/my_file.dat” you can add “sub_directory” as a folder/directory

- **Use “Edit CFLAGS…”**
  - To add any C compile flags required for compilation
Test benches I

- The test bench should be in a separate file
- Or excluded from synthesis
  - The Macro __SYNTHESIS__ can be used to isolate code which will not be synthesized
    - This macro is defined when Vivado HLS parses any code (-D__SYNTHESIS__)

```c
#include <stdio.h>
void test (int d[10]) {
    int acc = 0;
    int i;
    for (i=0;i<10;i++) {
        acc += d[i];
        d[i] = acc;
    }
    ifndef __SYNTHESIS__
    int main () {
        int d[10], i;
        for (i=0;i<10;i++) {
            d[i] = i;
        }
        test(d);
        for (i=0;i<10;i++) {
            printf("%d %d\n", i, d[i]);
        }
        return 0;
    } endif
```

Test benches II

- Ideal test bench
  - Should be self checking
    - RTL verification will re-use the C test bench
  - If the test bench is self-checking
    - Allows RTL Verification to be run without a requirement to check the results again
  - RTL verification "passes" if the test bench return value is 0 (zero)
    - Actively return a 0 if the simulation passes

```c
int main () {
    // Compare results
    int ret = system("diff --brief -w test_data/output.dat test_data/output.golden.dat");
    if (ret != 0) {
        printf("Test failed !!!\n", ret);
        return 1;
    } else {
        printf("Test passed !\n", ret);
        return 0;
    }
}
```

- Non-synthesizable constructs may be added to a synthesize function if __SYNTHESIS__ is used

```c
#ifndef __SYNTHESIS__
image_t *yuv = (image_t *)malloc(sizeof(image_t));
#else // Workaround malloc() calls without changing rest of code
image_t _yuv;
#endif
```
Solution Configuration

- **Provide a solution name**
  - Default is solution1, then solution2 etc.

- **Specify the clock**
  - The clock uncertainty is subtracted from the clock to provide an “effective clock period”
  - Vivado HLS uses the “effective clock period” for Synthesis
  - Provides users defined margin for downstream RTL synthesis, P&R

- **Select the part**
  - Select a device family after applying filters such as family, package and speed grade (see next slide)

Selecting Part and Implementation Engine

- **Select the target part either through Parts or Boards specify**

- **Select RTL Tools**
  - Auto
    - Will select Vivado for 7 Series and Zynq devices
    - Will select ISE for Virtex-6 and earlier families
  - Vivado
  - ISE
    - ISE Design Suite must be installed and must be included in the PATH variable
Clock Specification

- **Clock frequency must be specified**
  - Only 1 clock can be specified for C/C++ functions
  - SystemC can define multiple clocks
- **Clock uncertainty can be specified**
  - Subtracted from the clock period to give an effective clock period
  - The effective clock period is used for synthesis
    - Should not be used as a design parameter
    - Do not vary for different results: this is your safety margin
  - A user controllable margin to account for downstream RTL synthesis and P&R

Clock Specification

- **Clock Period**
- **Clock Uncertainty**
- **Effective Clock Period used by Vivado HLS**
- **Margin for Logic Synthesis and P&R**

---

A Vivado HLS Project

- **Project Explorer**
  - Project files displayed in a hierarchical view
- **Information Pane**
  - Can view and edit any file from the Project Explorer
- **Auxiliary Pane**
  - Cross-referenced with the Information Pane (here it shows objects in the source code)
- **Console Pane**
  - Displays Vivado HLS runtime messages
Vivado HLS GUI Toolbar

The primary commands have toolbar buttons

- Easy access for standard tasks
- Button highlights when the option is available
  - E.g. cannot perform C/RTL simulation before synthesis

Create a new Project
Create a new Solution
Change Project Settings
Change Solution Settings
Run C Simulation
Open Analysis Viewer
Compare Reports
Open Reports
Export RTL
Run C/RTL Cosimulation
Run C Synthesis

Files: Views, Edits & Information

Open file and it will display in the information pane

The Auxiliary pane is context sensitive with respect to the information pane
Here it displays elements in the code which can have directives specified on them
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Synthesis

- Run C Synthesis
- Console
  - Will show run time information
  - Examine for failed constraints
- A “syn” directory is created
  - Verilog, VHDL & SystemC RTL
  - Synthesis reports for all non-inlined functions
- Report opens automatically
  - When synthesis completes
- Report is outlined in the Auxiliary pane
Vivado HLS: RTL Verification

- RTL output in Verilog, VHDL and SystemC
- Automatic re-use of the C-level test bench
- RTL verification can be executed from within Vivado HLS
- Support for Xilinx simulators (XSim and ISim) and 3rd party HDL simulators in automated flow

RTL Verification: Under-the-Hood

- **RTL Co-Simulation**
  - Vivado HLS provides RTL verification
  - Creates the wrappers and adapters to re-use the C test bench

  - Prior to synthesis
    - Test bench
    - Top-level C function

  - After synthesis
    - Test bench
    - SystemC wrapper created by Vivado HLS
    - SystemC adapters created by Vivado HLS
    - RTL output from Vivado HLS
      - SystemC, Verilog or VHDL

- There is no HDL test bench created
RTL Verification Support

- **Vivado HLS RTL Output**
  - Vivado HLS outputs RTL in SystemC, Verilog and VHDL
    - The SystemC output is at the RT Level
    - The input is not transformed to SystemC at the ESL

- **RTL Verification with SystemC**
  - The SystemC RTL output can be used to verify the design without the need for a HDL simulator and license

- **HDL Simulation Support**
  - Vivado HLS supports HDL simulators on both Windows & Linux
  - The 3rd party simulator executable must be in OS search path

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C/RTL Co-simulation

- **Start Simulation**
  - Opens the dialog box

- **Select the RTL**
  - SystemC does not require a 3rd party license
  - Verilog and VHDL require the appropriate simulator
    - Select the desired simulator
  - Run any or all

- **Options**
  - Can output trace file (VCD format)
  - Optimize the C compilation & specify test bench linker flags
  - The “setup only” option will not execute the simulation

- **OK will run the simulator**
  - Output files will be created in a “sim” directory
Simulation Results

- Simulation output is shown in the console
- Expect the same test bench response
  - If the C test bench plots, it will with the RTL design (but slower)
- Sim Directory
  - Will contain a sub-directory for each RTL which is verified
- Report
  - A report is created and opened automatically

Vivado HLS: RTL Export

- RTL output in Verilog, VHDL and SystemC
- Scripts created for RTL synthesis tools
- RTL Export to IP-XACT, SysGen, and Pcore formats
- IP-XACT and SysGen => Vivado HLS for 7 Series and Zynq families
  PCore => Only Vivado HLS Standalone for all families
**RTL Export Support**

**RTL Export**
- Can be exported to one of the three types
  - IP-XACT formatted IP for use with Vivado System Edition (SE)
    - 7 Series and Zynq families only
  - A System Generator IP block
    - 7 Series and Zynq families only
  - Pcore formatted IP block for use with EDK
    - 7 Series, Zynq, Spartan-3, Spartan-6, Virtex-4/5/6 families

**Generation in both Verilog and VHDL for non-bus or non-interface based designs**

**Logic synthesis will automatically be performed**
- HLS license will use Vivado RTL Synthesis

---

**RTL Export: Synthesis**

**RTL Synthesis can be performed to evaluate the RTL**
- IP-XACT and System Generator formats: Vivado synthesis performed
- Pcore format: ISE synthesis is performed

**RTL synthesis results are not included with the IP package**
- Evaluate step is provided to give confidence
  - Timing will be as estimate (or better)
  - Area will be as estimated (or better)
- Final RTL IP is synthesized with the rest of the RTL design
  - RTL Synthesis results from the Vivado HLS evaluation are not used
RTL Export: IP Repositories

- IP can be imported into other Xilinx tools

**In Vivado:**
1. Project Manager > IP Catalog
2. Add IP to import this block
3. Browse to the zip file inside “ip”

**In System Generator:**
1. Use XilinxBlockAdd
2. Select Vivado_HLS block type
3. Browse to the solution directory

**In EDK:**
1. Copy the contents of the “pcore” directory
2. Paste into the EDK project pcore directory
3. Project > Rescan Local Repository

Solution directories:
There can be multiple solutions for each project. Each solution is a different implementation of the same (project) source code.

RTL Export for Implementation

- Click on Export RTL
  - Export RTL Dialog opens
- Select the desired output format
- Optionally, configure the output
- Select the desired language
- Optionally, click on Evaluate button for invoking implementation tools from within Vivado HLS
- Click OK to start the implementation
RTL Export (Evaluate Option) Results

- **Impl directory created**
  - Will contain a sub-directory for each RTL which is synthesized

- **Report**
  - A report is created and opened automatically

  ![Export Report for 'dct'](image)

  **General Information**
  - Device target: xc7z020clg484-1
  - Implementation tool: Xilinx Vivado v2013.3

  **Resource Usage**
  - VHDL: 89
  - LUT: 279
  - FF: 134
  - DSP: 1
  - RAM: 5
  - BRAM: 0
  - SRL: 0

  **Final Timing**
  - CP required: 10.000
  - CP achieved: 6.192

  ![Timing met](image)

RTL Export Results (Evaluate Option Unchecked)

- **Impl directory created**
  - Will contain a sub-directory for both VHDL and Verilog along with the ip directory

- **No report will be created**

- **Observe the console**
  - No packing, routing phases

  ![Observe the console](image)

Using Vivado HLS 12.3 - 30 © Copyright 2013 Xilinx
Outline

- Invoking Vivado HLS
- Project Creation using Vivado HLS
- Synthesis to IPXACT Flow
- Design Analysis
- Other Ways to use Vivado HLS
- Summary

Analysis Perspective

- Perspective for design analysis
  - Allows interactive analysis
Performance Analysis

Resources Analysis
Command Line Interface: Batch Mode

Vivado HLS can also be run in batch mode
- Opening the Command Line Interface (CLI) will give a shell

- Supports the commands required to run Vivado HLS & pre-synthesis verification (gcc, g++, apcc, make)
Using Vivado HLS CLI

- **Invoke Vivado HLS in interactive mode**
  - Type Tcl commands one at a time
    ```
    > vivado_hls -i
    ```

- **Execute Vivado HLS using a Tcl batch file**
  - Allows multiple runs to be scripted and automated
    ```
    > vivado_hls -f run_aesl.tcl
    ```

- **Open an existing project in the GUI**
  - For analysis, further work or to modify it
    ```
    > vivado_hls -p my.prj
    ```

- **Use the shell to launch Vivado HLS GUI**
  ```
  > vivado_hls
  ```

Using Tcl Commands

- **When the project is created**
  - All Tcl command to run the project are created in script.tcl
    - User specified directives are placed in directives.tcl
    - Use this as a template from creating Tcl scripts
      - Uncomment the commands before running the Tcl script

Help

Help is always available
- The Help Menu

In interactive mode
- The help command lists the man page for all commands

Outline

- Invoking Vivado HLS
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Summary

- Vivado HLS can be run under Windows XP, Windows 7, Red Hat Linux, and SUSE OS
- Vivado HLS can be invoked through GUI and command line in Windows OS, and command line in Linux
- Vivado HLS project creation wizard involves
  - Defining project name and location
  - Adding design files
  - Specifying testbench files
  - Selecting clock and technology
- The top-level module in testbench is main() whereas top-level module in the design is the function to be synthesized

Summary

- Vivado HLS project directory consists of
  - *.prj project file
  - Multiple solutions directories
  - Each solution directory may contain
    - impl, synth, and sim directories
    - The impl directory consists of pcores, verilog, and vhdl folders
    - The synth directory consists of reports, systemC, vhdl, and verilog folders
    - The sim directory consists of testbench and simulation files
Lab1 Intro
Vivado HLS Design Flow

Vivado HLS 2013.3 Version
ZedBoard

Objectives

After completing this lab, you will be able to:

- Create a project in Vivado HLS
- Run C-simulation
- Use debugger
- Synthesize and implement the design using the default options
- Use design analysis perspective to see what is going on under the hood
- Understand and analyze the generated output
The Design

This lab uses a simple matrix multiplication example to walk you through the Vivado HLS project creation and analysis steps. The design consists of three nested loops. The Product loop is the innermost loop performing the actual elements product. The Col loop is the outer-loop which feeds next column element data with the passed row element data to the Product loop. Finally, Row is the outer-most loop. The res[i][j]=0 (line 79) resets the result every time a new row element is passed and new column element is used.

```
#include "matrixmul.h"

void matrixmul(
    mat_t a[MAT_A_ROWS][MAT_A_COLS],
    mat_t b[MAT_B_ROWS][MAT_B_COLS],
    result_t res[MAT_A_ROWS][MAT_B_COLS])
{
    // Iterate over the rows of the A matrix
    for(int i = 0; i < MAT_A_ROWS; i++) {
        // Iterate over the columns of the B matrix
        for(int j = 0; j < MAT_B_COLS; j++) {
            // Do the linear product of a row of A and col of B
            res[i][j] = 0;
            for(int k = 0; k < MAT_B_ROWS; k++) {
                res[i][j] += a[i][k] * b[k][j];
            }
        }
    }
}
```

Procedure

- Create a project after starting Vivado HLS in GUI mode
- Run C simulation
  - to understand the design behavior
- Run the debugger
  - to see how the top-level module works
- Synthesize the design
- Analyze the generated output using the Analysis perspective
- Run C/RTL cosimulation
  - to perform RTL simulation
- View simulation results in Vivado
  - to understand the IO protocol
- Export RTL in the Evaluate mode and run the implementation
In this lab, you completed the major steps of the high-level synthesis design flow using Vivado HLS. You created a project, added source files, synthesized the design, simulated the design, and implemented the design. You also learned that how to use the Analysis perspective to understand the scheduling.