EE 382M
VLSI–II
Class Overview
Fall 2008

Mark McDermott
EE 382M VLSI - II

• Instructor(s):
  – Peter Hofstee, Kevin Nowka, Byron Krauter, Gian Gerosa, Steve Sullivan, Matt Amatangelo, Hector Sanchez, Jerry Moench, Romi Datta
  – Mark McDermott
    • Office: ENS 425
    • Office hours: By appointment

• TA’s:
  – Eun Jung Jang

• Prerequisite: Graduate VLSI-I, logic design, basic computer architecture.

• Web URL: http://www.ece.utexas.edu/~mcdermot/
• Lecture notes, homework, exercises will be posted on the web.
Do’s and Don’ts

• **Do’s**
  – Update your email address on Blackboard and in ECE.
  – Show up for class on time. Class starts promptly at 8:00 and will end as close to 12:00 as possible
  – Read the lecture notes before coming to class and ask lots of questions
  – Show up for group office hours

• **Don’ts**
  – Leave your cell phone on during class.
Goals of this class

This class will introduce you to the tools that are needed to solve VLSI design planning, circuit design and integration problems. There will be 4 homework problems and a team class project which will help you to practice using these tools and techniques. The class provides examples of current design techniques, so that you can evaluate them and come to your own conclusions about their application to the real world. This experimentation will help you with building the foundation you need, to choose the appropriate circuits and simulation methods to solve your problems.
Design of SOC Systems

- Algorithms
- System: HW & SW
- Macro Components
- Cells

MS System Design

Analog-2

SOC System Design

VLSI-II

Analog-1

VLSI-I

System Level

Top-down Passing constraints

Bottom-Up Feedback

Cell Level
Design Phases

Early Phase:
Design Planning
- Estimated

Mid Phase:
Design Construction
- Mixed
- Structured Netlist
- Mapped Netlist

Late Phase:
Design Tuning
- Extracted
- Schematic Netlist
- Consistency
- Partial
- Full

Design Database

Netlist
- Layout

Cell Libraries
- Design Specs & Netlist
Suggested Reading

- Harris, *Skew Tolerant Circuit Design*, Morgan Kaufmann Publishers
- Bakoglu, *Circuits, Interconnections and Packaging for VLSI*, Addison Wesley
Homework

- Homework is designed for you to get experience with DSM technology and simulation and to experiment with new design techniques.
- HW Problems are posted on the web and are due in about 4 weeks. Problems MUST be worked out on your own. DO NOT share your work.
- No late assignments - Late submission of homework and lab exercises will result in a 25% penalty per day. (Max penalty: 100% - Yes it is tough, but so is the real world). HW must be submitted at the beginning of class.
- Other homework you must do: Read the course notes. Be prepared before coming to class.
Class Project

• **Project assignment:**
  Project is focused on the early design planning, timing and optimization of an “Open Cores” processor core. Project will be reviewed during the last 2 days of the class.
Exams & Grading

• There will be two exams. Due to the flow of the class I cannot change these dates for any reason.
  – Oct 18th
  – Nov 15th

• Both exams are in class, closed notes, closed book, closed notebook computer, closed iPhone, etc.

• Class Project design review: last 3 weeks of class

• Grading:
  – Homework: 40%
  – Exam 1: 15%
  – Exam 2: 15%
  – Final Project: 30%
Caveats (courtesy of Mark Horowitz)

• Never take anything on blind faith. Work it out -- make sure it works. Many clever circuits that are published either don’t work or are very sensitive to certain conditions. Be careful.

• There are NO RIGHT answers, and there are no PERFECT circuits. Everything has its warts. A good circuit simply has the right set of warts to meet the constraints of the problem.

• Simulation is NO substitute for thinking. HSPICE can make your job much easier, but it also can make it incredibly harder. Like all tools it helps only if you use it well, AND that requires thinking. Work it out on paper and then let HSPICE validate it.

• DO NOT BECOME a SLAVE to the TOOLS. Tools can tell you wrong answers.
Collaboration is good! Cheating is not good!

• **Collaboration** is good!
  – Discussing issues with your classmates is a good way to learn and a study group is a very effective learning tool
  – Helping each other learn is particularly satisfying
  – **But**....*Individual assignments and exams must be done by individuals*

• Cheating is a serious breach of trust and will not be tolerated
  – If ever in doubt, don’t do it or ask me immediately for a clarification
    • See University Policies for further detail
  – Take some free advice from me: Don’t cheat, its not worth it