EE 382M
VLSI–II: Advanced Circuit Design
Noise Analysis

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Outline

- General Remarks
  - Timing Failures vs. Noise Failures
  - Frequency Dependent Noise Failures
  - Fixing Noise Failures
  - Noise Analysis
- Circuit Sensitivity
- Cross Talk Noise
- Common Mode Noise
- Power Supply Noise
- Leakage Currents
- Miscellaneous Noise
- Domino Noise Solutions
- Summary
Timing & Noise Failures

• Timing Failures
  – Occur when noise impacts a long path delay
    • Noise is injected on switching nets & circuits
  – Hardware functions correctly with a slower clock
  – Design changes required to achieve highest clock rates, but chip will operate at slower frequency

• Noise failures
  – Occur when noise disrupts a quiet logic state
    • Injected noise arrives at latch when latch is sampled
    • Some failures resolve with slower clock
    • Some failures are independent of clock rate
    • Some failures brought on at slower clock rates
    • Some failures change with voltage & temperature
  – Design changes are required to achieve any functionality
Timing Failure Example

Aggressor & victim switch simultaneously (in opposite directions) & victim net is in critical path!

 clk
    
 aggressor

    victim

 clk

 critical path

 clk

 clk

 aggressor

 victim
Noise Failure Example I

Victim net is not in critical path but late aggressor noise pulse propagates down the victim net & arrives at latch at sampling time.

Functional with slower clock because noise arrives after latch is sampled.
Noise Failure Example II

If OR gate is a dynamic circuit that evaluates when clk=0, then a much slower clock is needed to restore functionality!

Functional with slower clock because noise pulse is pinned to a different clock phase.
Noise Failure Example III

If dynamic OR gate evaluates and aggressor launches on same clock phase, a slower clock won’t make the hardware function!

Noise pulse and dynamic OR evaluate locked in same half cycle
Frequency Dependent Noise Failures

![Diagram of Frequency Dependent Noise Failures](image-url)
Frequency Dependent Noise Failures

All latches master-slave at a single frequency

Aggressor Window

Victim Window
Frequency Dependent Noise Failures

All latches master-slave at a single frequency

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Aggressor Window

Victim Window
Fixing Noise Failures

• Reduce noise level below circuit noise sensitivity
  – Changes might include:
    • Wiring changes
    • Power distribution changes
    • Power gating settings
    • Aggressor circuit or keeper circuit changes
    • Clock or timing changes
  – Invariably costs additional design resource
• Increase circuit noise sensitivity above noise level
  – Involves some type of circuit change
    • Dynamic to static
    • Different p/n ratio
    • Hysteresis feedback loops
    • Larger keeper devices on domino gates
  – Invariably trades speed for increased noise immunity
Noise Analysis

Noise is typically analyzed as individual driver-receiver pairs. Accounts for both noise generation and noise reception!

A budget for total noise prevents failure at this receiver. A budget for propagated noise prevents failure at the next receiver.
Circuit Sensitivity
A gate’s noise margins are formally defined by the unity gain points of its transfer curve.

\[ \text{UNM}(h) = V_{ouh} - V_{iuh} \]
\[ \text{UNM}(l) = V_{iul} - V_{oul} \]

The unity gain noise margins are the maximum amounts of DC noise which can be added to every node.

DC measurements of noise and noise margins tend to be overly conservative.
Adjust P/N Ratio of Receiver

Changing the P/N ratio of a receiver can greatly affect its sensitivity to noise.

Con: May slow critical transition
Circuit Noise Margins

AC Noise Immunity

positive noise

gnd

pulse height

pulse width

unsafe

vdd

safe

negative noise

vdd

gnd

pulse height

pulse width

safe

unsafe
Lower Fan-In of Receiver

Low fan-in gates after noisy nodes will attenuate noise before sensitive receivers are reached.  

Con: Can increase delay
Reduce Size of Receiver

Smaller sized receiver will respond more slowly to transient noise.

Con: Increases delay
Size Up Driver or Keeper

A larger driver or keeper will provide more current to hold a node at its proper value.

Con: Increases area
     Increases power
CrossTalk
CrossTalk (Coupling) Noise

A changing voltage on any wire affects the voltage of surrounding wires.

\[ V_{\text{Worst case noise bump}} = V_{cc} \left( \frac{C_{ll}}{C_{tot}} \right) \]

General CrossTalk Solutions:
- Decrease capacitance to aggressors
- Increase capacitance to non-aggressors
- Increase driver strength or reduce wire resistance

\[ C_{tot} = \text{total capacitance of victim node} \]
\[ C_{ll} = \text{capacitance to aggressors} \]
Change Floorplan to Reduce Wire Length

Shorter wire length decreases aggressor capacitance.

Good floorplan can greatly reduce the distance traveled by noisy signals.  

Con: May make other wires longer
Shield Victim Signals

Shielding reduces aggressor capacitance

**Con:** Can use more wiring tracks
Increase Wire Spacing

Increased wire spacing reduces aggressor capacitance.

Con: Uses more wiring tracks
Increase Wire Width

Wider wire reduces resistance and increases non-aggressor capacitance.

Con: Uses more wiring tracks
Use Higher Metal Layer

Higher level metals are thicker and therefore have less resistance.

Con: Takes tracks from global routes Total and aggressor capacitance are about the same.
HW 6: Cross-Talk Schematic

Measure noise at input to I4

Vdd
Add Repeaters

Inverters are very effective at filtering out noise.

**Con:**
- Increases area
- Can increase delay
Slow Attacking Signals

**Con:** Can cause maxdelay failures
Aggressor signals become noise sensitive

Slower slew rate on aggressors allows more time for victim’s driver to supply current.
Twisted Differential Buses

Aggressors which are complements of each other cancel out.

Con: Uses extra metal layers
Complicates layout
Capacitive Cross Talk in Static Timing Analysis

- Static timing analysis reduces coupled circuit models into uncoupled models

\[ C_{10} \quad \alpha C_{12} \quad C_{20} \]

- What’s the worst case \( \alpha \)? Early mode & late mode.
Capacitive Cross Talk in Static Timing Analysis

- Switching on a balanced receiver occurs at $\frac{1}{2} V_{dd}$
- To find $\alpha$ solve $dQ = C*dV$ for $C_{12}$

<table>
<thead>
<tr>
<th></th>
<th>Earliest</th>
<th>Early</th>
<th>Nominal</th>
<th>Late</th>
<th>Latest</th>
</tr>
</thead>
<tbody>
<tr>
<td>Line 1 activity</td>
<td></td>
<td></td>
<td>$0 - V_{dd}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$\tau_r = t_1$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Line 2 activity</td>
<td></td>
<td></td>
<td>quiet</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$dV$ on $C_{12}$</td>
<td></td>
<td></td>
<td>$\frac{1}{2} V_{dd}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\alpha$</td>
<td></td>
<td></td>
<td>1</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Common Mode Noise
Common Mode Noise

- Interconnect return currents closely follow signal lines at high frequencies
  - Minimizes the loop inductance and total loop impedance

- Simultaneous switching of wide busses creates common mode noise on signals parallel to bus
  - Low impedance signals carry some of the return current

- Common mode noise has both inductive and resistive components

- Can add or subtract from capacitive crosstalk
  - Same transition adds to capacitive crosstalk at near end
  - Same transition subtracts from capacitive crosstalk at far end
Common Ground RC Interconnect Model
RC Interconnect Model with Return Paths
Effect of N Circuits Switching Simultaneous
Common Mode Noise Measurements

circa 1999
130 nm
Common Mode Noise Measurements

Far End Noise

Near End Noise

long wire
1.30 mm (wafer) reset_b

short wire
0.70 mm (wafer) reset_b

clk

Set Reset Latch

Set Reset Latch
Common Mode Noise Measurements

dc switch points
with Vdd = 1.5 Volts and T = 60 degrees

Low Vt -> 0.280 Volts
High Vt -> 0.428 Volts
Common Mode Noise Measurements

M7

M6

M5

M4

M3

M2

M1

noise sensitive line #1

noise sensitive line #2
Common Mode Noise Measurements

Table 1: CrossTalk Fails

<table>
<thead>
<tr>
<th>Receiver Threshold</th>
<th>Driver Strength</th>
<th>Line Length</th>
<th>Location</th>
<th>Total Fails</th>
</tr>
</thead>
<tbody>
<tr>
<td>LT</td>
<td>HT</td>
<td>4</td>
<td>8</td>
<td>12</td>
</tr>
<tr>
<td>00x00 01x00</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>00x00 11x00</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>00x00 10x11</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>00x00 01x10</td>
<td>16</td>
<td>7</td>
<td>17</td>
<td>5</td>
</tr>
<tr>
<td>10x01 01x10</td>
<td>6</td>
<td>4</td>
<td>10</td>
<td>0</td>
</tr>
<tr>
<td>00x00 01x11</td>
<td>23</td>
<td>14</td>
<td>23</td>
<td>8</td>
</tr>
</tbody>
</table>

Table 2: Simultaneous Switching Fails

<table>
<thead>
<tr>
<th># of Lines Switching 0 -&gt; 1</th>
<th># of Lines Switching 1 -&gt; 0</th>
<th>Receiver Threshold</th>
<th>Driver Strength</th>
<th>Line Length</th>
<th>Location</th>
<th>Total Fails</th>
</tr>
</thead>
<tbody>
<tr>
<td>LT</td>
<td>HT</td>
<td>4</td>
<td>8</td>
<td>12</td>
<td>16</td>
<td>L</td>
</tr>
<tr>
<td>40</td>
<td>600</td>
<td>24</td>
<td>15</td>
<td>22</td>
<td>8</td>
<td>1</td>
</tr>
<tr>
<td>20</td>
<td>20</td>
<td>23</td>
<td>14</td>
<td>23</td>
<td>8</td>
<td>0</td>
</tr>
<tr>
<td>320</td>
<td>320</td>
<td>22</td>
<td>13</td>
<td>22</td>
<td>7</td>
<td>6</td>
</tr>
<tr>
<td>320</td>
<td>0</td>
<td>25</td>
<td>12</td>
<td>22</td>
<td>7</td>
<td>6</td>
</tr>
<tr>
<td>640</td>
<td>0</td>
<td>23</td>
<td>11</td>
<td>21</td>
<td>7</td>
<td>4</td>
</tr>
</tbody>
</table>

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Power Supply Noise
Power Supply Noise

- Power Supply Noise = Z * I
  - Global noise
    - Function of total chip switching, chip power grid, chip decoupling capacitance & chip packaging
    - Δt > couple of clock cycles
  - Local noise
    - Function of local circuit switching, local power grid & local decoupling capacitance
    - Δt < clock cycle

- Ratio of Noise to Supply Voltage Is Increasing
  - \( V_{\text{noise}} = Z \times I = Z \times \frac{P}{V_{\text{supply}}} \)
  - Consider fixed power density (P) and impedance (Z)
  - Scaling yields a worsening \( \frac{V_{\text{noise}}}{V_{\text{supply}}} = \frac{Z \times P}{(V_{\text{supply}})^2} \)
Global Power Supply Noise
Chip/Package Resonance

- Chip/package forms an LRC tank circuit
- Driving point has a resonant impedance
  - \[ 2\pi f_{\text{res}} \approx (LC)^{-1/2} \]
    - \( L = L_{\text{package}} + L_{\text{board}} + L_{\text{cap}} \)
    - \( C = \text{Chip capacitance} \)
  - \( Z(f_{\text{res}}) \) is a function of Q
- Increasing chip power always decreases \( Z(f_{\text{res}}) \)
  - DC power
    - Nonlinear subthreshold leakage is even better!
  - Constant AC power (e.g. free running clocks)
Two Pole Model Perspective

\[
Z(s) = \frac{R_c(s + \frac{1}{R_cC})(s + \frac{R_i}{L})}{s^2(1+\alpha) + s\left(\frac{(R_c + (1+\alpha)R_i)}{L} + \frac{1}{R_oC}\right) + \frac{(1+\beta)}{LC}}
\]

where \(\alpha = \frac{R_c}{R_o} \ll 1\), \(\beta = \frac{R_i}{R_o} \ll 1\)

Approximate Behavior

\[
2\pi f_{res} \approx (LC)^{-1/2}
\]

\[
Z(f_{res}) \approx \frac{L}{(R_i + R_c)C + \frac{L}{R_o}}
\]

for \(\frac{R_i}{L} \ll (LC)^{-1/2} \ll \frac{1}{R_cC}\)
Hardware Measurements

• Driving point impedances indirectly measured at IBM*, Intel .. using clock/power gating & Ohm’s law

\[ Z(f) = \frac{V(f)}{I(f)} = \frac{F(V(t))}{F(I(t))} \]

• V(f) measured with spectrum analyzer & I(f) approximated by Fourier component of stimulus

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Cell Chip/Package Measurements

Initial Cell chip on a 4-2-4 Organic package with 35 “0508” decaps. Non-Optimal board

170MHz

Power 5 Chip/Package Measurements
With & Without On-chip Capacitance @L2CNTL

Power 5 Chip/Package Measurements

Correlation with Chip-Package Resonance Frequency

Parent 0422: WITH onchip cap  
$$\frac{1}{2 \times 6.5\text{nsec}} = \sim 77\text{Mhz}$$
Power 5 Chip/Package Measurements
Correlation with Chip-Package Resonance Frequency

Child 9046: NO onchip cap \( f = \frac{1}{2 \times 4 \text{nsec}} = \sim 125 \text{Mhz} \)

Chip/Package Noise Is Not New

- First dealt with resonant chip/package noise in late 80’s
  - Clock frequency was approaching chip/package resonant frequency
  - Step response overshoot was reducing burn-in yields

- 1\textsuperscript{st} harmonic concerns receded when chip frequencies began passing resonant frequencies
  - Faster clocks meant less noise
Chip/Package Noise Is Not New

- First PowerPC chips quieter at higher frequencies
Chip/Package Noise Is Not New

- **Step response remained a concern & sometimes hurt power gating efforts**
  - **Power2** (8 chip) MCM (circa 1993)
    - Coarse clock gating domains (e.g. data cache access)
    - Data cache gating on 4 chips reduced power 30 Watts
    - Data cache gating disabled to improve sort yield at $f_{\text{max}}$
  - **Power5** (8 chip) MCM (circa 2003)
    - Fine grain clock gating domains
    - Disabled on a small FPU unit (in CPUs) to improve yield at $f_{\text{max}}$
    - Power increased by a few milliwatts
Local Power Supply Noise
Local IR Noise

Local iR drops occur when power mesh is neglected

![Circuit Diagram]

![Waveform]
Local AC Noise

Local supply variations within a cycle reduce dynamic circuit margins & half cycle paths

![Diagram of electric circuits and waveforms](image)
Local Step Response Noise

- Chip/Package more complex than a 2 pole model
- Distributed model includes lateral impedances
  - Chip lateral impedance is highly resistive (and is often ignored)
  - Package lateral impedance is inductive & resistive
- Local switching creates
  - Local noise $\propto Z_{11}$ (driving point impedance)
  - Remote noise $\propto Z_{12}$ (transfer impedance)
- Local noise radially propagates at velocity $v = (LC)^{-1/2}$
  - $L =$ package lateral inductance (Henrys per square)
  - $C =$ chip decoupling capacitance (Farads per unit area)
- Propagation delay across chip greater than cycle time
  - Staggered step response $\Rightarrow$ worst case switching event
Local Power Supply Noise

Local IR noise
  Minimize power grid resistance
  Connect all orthogonal power crossovers
  Minimize total circuit current

AC noise: All of the above plus
  Minimize current transients
  Physically & temporally spread out switching
  Add decoupling capacitors

Local step response: All of the above plus
  Minimize power supply inductance
  Include programmable fine grain clock gating
Increase Number of Power Lines

Reduces both resistance and inductance of power grid.

Con: Reduces tracks available for signals
Increase Width of Power Lines

Reduces resistance of power grid.

Con: Reduces tracks available for signals
Add Decoupling Capacitors

Capacitors added to power grid can provide charge for current transients.

Con: Layout effort
Total benefit uncertain
Reduce Size of Huge Drivers

Distributing huge drivers allows current to be drawn from larger area of power grid.

Con: Adds wire load

Rule of Thumb: Max effective width of 100um for PMOS and 50um for NMOS
Reduce Size of Wide Bus Drivers

Small drivers on very wide buses can cause large transient currents.

Con: Adds delay
Weak driver can lead to failure at receiver

Adding repeaters can reduce size of needed driver without increasing delay.
Split Timing of Wide Bus Drivers

For extremely large buses (>128 bits) driving at slightly different times can greatly reduce the induced supply noise.

Con: Bits of bus do not all arrive at the same time.
Leakage Noise
Subthreshold Leakage

For $V_{gs} < V_{t}$, drain to source current is not actually zero.

Subthreshold Slope $\approx 80-100$ mV/decade

Leakage currents prevent gates from making full rail swings

Subthreshold leakage is particularly bad in gates with many parallel devices.
Avoid Gates with Many Parallel Paths

Wide fan-in gates are susceptible to all forms of noise including subthreshold leakage

Con: May limit logic in next gate

Using Low Vt devices increases subthreshold current dramatically.
Gate Leakage

Electron’s position is not well defined and for oxides less than 5nm thick, tunneling current through the oxide can be significant.

Gate leakage is particularly bad in gates driving many receivers.
Avoid undersizing gates with large fanouts

Very weak drivers are susceptible to all forms of noise including gate leakage.

Con: Increased area and power
Miscellaneous Noise
Weakly held nodes can be disturbed by gate to drain capacitance, dramatically increasing gate delay.

Make sure weakly held nodes are not connected to top device of a series stack.
Setup & Hold Noise

Latch nodes with little margin for setup or hold time will have added noise.

Budget for extra noise on latch nodes and avoid designs which will add even more.
Soft Error Rate (SER)

Neutrons from cosmic rays acts as sites of electron-hole pair generation.

Sufficient charge can cause low capacitance state nodes to flip.

Solutions to SER:

• Maintain minimum capacitance on every node
• Add parity or ECC to large memory arrays
• Use Silicon on Insulator (SOI)
Domino Noise Solutions
Increase Keeper Size

Up to a point noise margin in any domino gate can be improved by increasing the keeper size.

Con: Increases delay and power
Sizing Keepers

\[ \text{NumN} \times \frac{\text{Wn}}{20} < \text{Wkpr} < \frac{\text{Wn}}{2} \]

Min keeper size set by noise requirements

\[ \text{Wkpr} < \frac{\text{Wn}}{2} \]

Max keeper size set by delay degradation

\[ \text{NumN} < 10 \]

Maximum noise sensitivity and delay limit number of parallel stacks.
Pseudo CMOS Input Protection

PMOS devices added to domino inputs precharge intermediate nodes and provides current in case of noise bump up on input.

**Con:** Increased load on inputs
Can’t be used for parallel paths
Charge Sharing

During evaluate A goes high while B stays low causing charge sharing between C1 and C2.

General Charge Sharing Solutions:
- Precharge intermediate node
- Decrease C2
- Increase C1

Out = \( V_{cc} \times \frac{C_2}{C_1 + C_2} \)
Intermediate Precharge Device

Extra PMOS device makes sure intermediate node is always precharged.

**Con:** Increased clock load
Select Signals on Top of Stack

With select signals at top of stack there can only be charge sharing to a single intermediate node.

Less diffusion load connected to output also leads to faster switching.
Symmetric Pulldown Stacks

Splitting stacks and reordering inputs cuts charge sharing in half.

Con: More complex layout
Increase Size of CMOS Receiver

Increased capacitance on dynamic node reduces impact of intermediate capacitance. **Con:** Increase dynamic gate delay

Smaller delay through CMOS gate may offset increased delay at this gate.
Summary
General Noise Learnings

• Can always trade speed for noise
• Less sensitive receiver much better than stronger driver
• Avoid extremely high or low slew rates
• Don’t plan on using minimum pitch wiring everywhere
• Domino requires extra design time & margin for noise
• Noise increases with increasing physical & temporal separation