EE-382M

VLSI–II

A brief summary of trends, device limitations, scaling, device performance in CMOS technologies

Gian Gerosa, Intel
Fall 2008
Transistors on a chip doubles every \(~2\) years.
Die Size Growth in Desktop/Mobile Processors (mm per side)

Per side (mm) ~7% growth per year

~2X growth in 10 years

Die size used to grow ~14% every two years
Logic Transistor Density

Shrinks & Compaactions meet density goals
New u-Architectures drop density

Courtesy: Shekhar Borkar, Intel
Each processor has several revisions

Time

1.5µ 1.0µ 0.8µ 0.6µ 0.35µ 0.25µ 0.18µ 0.13µ

80386
80846
Pentium
Pentium II,III
Pentium 4
Frequency used to double every \( \sim 2 \) years

POWER WALL at \( \sim 100 \text{W} \) stopped this.
Power Dissipation of Compactions

Lead processor power increases. Compactions provide higher performance at lower power.

Courtesy: Shekhar Borkar, Intel
Power Dissipation of Lead uP

Power (Watts)

<table>
<thead>
<tr>
<th>Year</th>
<th>Power</th>
</tr>
</thead>
<tbody>
<tr>
<td>1971</td>
<td>4004</td>
</tr>
<tr>
<td>1974</td>
<td>8008</td>
</tr>
<tr>
<td>1978</td>
<td>8080</td>
</tr>
<tr>
<td>1985</td>
<td>8085</td>
</tr>
<tr>
<td>1992</td>
<td>286</td>
</tr>
<tr>
<td>2000</td>
<td>486</td>
</tr>
</tbody>
</table>

Power increases exponentially

Courtesy: Shekhar Borkar, Intel
Effects of Scaling

![Graph showing the relationship between Power (Watts) and Clock Frequency (MHz) for different Intel processors over time. The graph illustrates the exponential growth in power consumption with increased clock frequency.]
90 nm CPU Chips

Prescott CPU

- 112 mm$^2$ die size
- 125 million transistors

Dothan CPU

- 87 mm$^2$ die size
- 144 million transistors

90 nm process now ramping on high performance CPU products

Source: Mark Bohr, Intel Corporation
MEROM core2 duo in 65nm

~180 mm²
~450 million transistors
PENRYN core2 duo in 45nm

~105 mm²
~510 million transistors
SILVERTHORNE (ATOM Processor) in 45nm

~25 mm²
~47 million transistors
Deep Sub-micron CMOS device Cross Section

- CoSi$_2$
- Halo Implant
- Si$_3$N$_4$
- S/D Extension
- P-Well
- N-Well
- P+ implant
- N+ implant
- Shallow trench isolation
- P-Epi
Deep Sub-Micron Transistors

- Characteristics in the linear, saturation, and sub-threshold regions
- Leakage
- Parasitic Elements
- Performance / Leakage tradeoff

130nm Generation

Courtesy: Mark Bohr, Intel

130nm Generation

70 nm
Feature Size Scaling

Transistor gate length is smaller than other features for improved performance and reduced power.

Source: Mark Bohr, Intel Corporation
Strained silicon increases electron/hole mobility.
65 nm Generation Transistors

- 35 nm gate length
- 1.2 nm gate oxide
- NiSi for low resistance
- 2^{ND} generation strained silicon for enhanced performance

Source: Mark Bohr, Intel Corporation
High-K, Metal Gate 45 nm CMOS (intel)

Strained Silicon Transistors

Intel’s unique strained silicon technology increases transistor drive current by an average of >30%

Source: Mark Bohr, Intel Corporation
SOURCES of TRANSISTOR LEAKAGE

Subthreshold Leakage

Junction Leakage

Gate Leakage

$I_{off}$

$I_{jctn}$

$I_{gate}$

Ilkg indicator = 0.5(ON state) + 0.5(OFF state)

= 0.5($I_{gate}$ (ON)) + 0.5($I_{off}$ + $I_{jctn}$ + $I_{gate}$ (OFF))
Transistor Leakage Components

Performance vs. Leakage Tradeoff

Performance vs Leakage:

\( V_T \downarrow I_{OFF} \uparrow I_D(SAT) \uparrow \)

\[
I_{OFF} \propto I_{subth} \propto \frac{W_{eff}}{L_{eff}} K_1 e^{(V_{GS}-V_T)}
\]

\[
I_D(SAT) \propto \frac{W_{eff}}{L_{eff}} K_2 (V_{GS}-V_T)^2
\]

\[
I_D(SAT) \propto K_3 W_{eff} C_{ox} \nu_{SAT} (V_{GS}-V_T)
\]

- As \( V_T \) decreases, sub-threshold leakage increases
- Leakage is a barrier to voltage scaling
65 nm Transistors
Ioff vs. Idsat

IEDM 2004, P. Bai et al., “A 65nm Logic Technology
Featuring 35nm Gate Length, Enhanced Channel
Strain, 8 Cu Interconnect Layers, Low-k ILD and
0.57um2 SRAM Cell”.

Record 1.46 mA/μm $I_{\text{DSAT}}$ at 1.2 V and 100 nA/μm $I_{\text{OFF}}$

Record 0.88 mA/μm $I_{\text{DSAT}}$ at 1.2 V and 100 nA/μm $I_{\text{OFF}}$
Deep Submicron Device PARASITICS

Source-Drain Resistance

Gate Resistance

Parasitic Capacitances

Constant Field Scaling

Some numbers .. Constant Electric Field Scaling

\[ Width = W = 0.7, \ Length = L = 0.7, \ t_{ox} = 0.7 \]

1. Lateral and vertical dimensions reduce 30%

\[ Area \ Cap = C_a = \frac{0.7 \times 0.7}{0.7} = 0.7, \quad \sim (e^*W^*L)/Tox \]

\[ Fringing \ Cap = C_f = 0.7, \quad \sim W \]

\[ Total \ Cap \Rightarrow C = 0.7 \]

2. Capacitance--area and fringing--reduce 30%

\[ Die \ Area = X \times Y = 0.7 \times 0.7 = 0.7^2 \]

3. Die area reduces 50%
Constant Electric Field Scaling –cnt’d-

\[
\frac{\text{Cap}}{\text{Transistor}} = \frac{0.7}{1} = 0.7
\]

4 Capacitance per transistor reduces 30%
\[
\frac{\text{Cap}}{\text{Area}} = \frac{0.7}{0.7 \times 0.7} = \frac{1}{0.7}
\]

5 Capacitance per unit area increases 43%

\[
V_{dd} = 0.7, V_t = 0.7, I = \frac{W}{t_{ox}} (V_{dd} - V_t) = \frac{0.7 \times 0.7}{0.7} = 0.7
\]

\[
T = \frac{C \times V_{dd}}{I} = \frac{0.7 \times 0.7}{0.7} = 0.7, \quad \text{Power} = C \times V^2 \times f = \frac{0.7 \times 0.7^2}{0.7} = 0.7^2
\]

6 Delay reduces 30%, power reduces 50%
### What About Constant Voltage Scaling?

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Before Scaling</th>
<th>After Full Scaling</th>
<th>After Constant Voltage Scaling</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel length</td>
<td>L</td>
<td>L/S</td>
<td>L/S</td>
</tr>
<tr>
<td>Channel width</td>
<td>W</td>
<td>W/S</td>
<td>W/S</td>
</tr>
<tr>
<td>Gate oxide thickness</td>
<td>( t_{ox} )</td>
<td>( t_{ox}/S )</td>
<td>( t_{ox}/S^* )</td>
</tr>
<tr>
<td>Junction Depth</td>
<td>( x_j )</td>
<td>( x_j/S )</td>
<td>( x_j/S )</td>
</tr>
<tr>
<td>Doping Densities</td>
<td>( N_A, N_D )</td>
<td>( S \cdot N_A, S \cdot N_D )</td>
<td>( S^2 \cdot N_A, S^2 \cdot N_D )</td>
</tr>
<tr>
<td>Power supply voltage</td>
<td>( V_{DD} )</td>
<td>( V_{DD}/S )</td>
<td>( V_{DD} )</td>
</tr>
<tr>
<td>Threshold Voltage</td>
<td>( V_{T0} )</td>
<td>( V_{T0}/S )</td>
<td>( V_{T0} )</td>
</tr>
</tbody>
</table>

* In some forms of constant voltage scaling \( t_{ox} \)
A comparison ......

**Constant voltage scaling**

\[
C = 0.7, V = 1 \\
I = \frac{W}{t_{ox}} (V - V_t) = \frac{0.7}{0.7} \times 1 = 1 \\
D = \frac{CV}{I} = \frac{0.7 \times 1}{1} = 0.7 \\
Power = CV^2F = \frac{0.7 \times 1}{0.7} \\
Power = 1 \\
Power Density = 1/0.7^2 = 2
\]

**Constant electric field scaling**

\[
C = 0.7, E = \frac{V}{t_{ox}} = \frac{0.7}{0.7} = 1, E = \frac{V}{L} = \frac{0.7}{0.7} = 1 \\
I = \frac{W}{t_{ox}} (V - V_t) = \frac{0.7}{0.7} \times 0.7 = 0.7 \\
D = \frac{CV}{I} = \frac{0.7 \times 0.7}{0.7} = 0.7 \\
Power = CV^2F = \frac{0.7 \times 0.7^2}{0.7} \\
Power = 0.5 \\
Power Density = 0.5/0.7^2 = 1
\]
Issues with Constant Voltage Scaling

- Practical (from the systems integration point of view), since the power supply and signal voltages are unchanged ...... but,
- **Electric field increases by factor** $k (1/S)$. Can cause transistor failures such as oxide breakdown, punch-through, and hot electron charging of the oxide.
- **Current density** will also increase in transistors as well as metals causing self-heating and metal migration in interconnects.
- **Power density** $(P/\text{area})$ is increasing causing localized heating and heat dissipation problems.
- In reality, CMOS technology evolution has followed a mixture of both constant field and constant voltage scaling.
Non-Scaling Effects

• Subthreshold Current: since $kT/q$ and $E_g$ do not scale ..... 

\[ I_{\text{off}} = \mu_{\text{eff}} C_{\text{ox}} \frac{W}{L} (\frac{kT}{q})^2 e^{-\frac{qV_t}{mkt}} \]

• The Polysilicon gate depletion contributes a Capacitance which is in series with the oxide capacitance $C_{\text{ox}}$ ..... Thus the total gate capacitance does not scale exactly to $1/K$ ..... unless metal gates are used.

• The full benefit of scaling cannot be realized unless process tolerances ($L_{\text{eff}}, T_{\text{ox}}, V_t$, etc.) scale along with $1/K$. 
Transistor Performance Trends

\[ Q = CV \]
\[ \frac{dQ}{dt} = C \frac{dV}{dt} \]
\[ i = C \frac{dV}{dt} \]
\[ dt = C \frac{dV}{i} \]

Delay = \[ \frac{CV}{I_{dsat}} \]
CMOS Inverter Delay

Using \( C \frac{dV}{dt} = i \)

\[
C_\text{-} \frac{d(V\text{out} - \phi)}{dt} + C_\text{+} \frac{d(V\text{out} - V\text{dd})}{dt} = -I_n
\]

\[
(C_\text{-} + C_\text{+}) \frac{dV\text{out}}{dt} = C \frac{dV\text{out}}{dt} = -I_n \quad \Rightarrow \quad \Delta t = \frac{C dV\text{out}}{-I_n}
\]

Inverter Delay -cnt'd-

\[ \tau_n = \frac{CV_{dd}}{2I_{NSAT}} = \frac{CV_{dd}}{2W_nI_{DSSN}} \]

Similarly,

\[ \tau_p = \frac{CV_{dd}}{2W_pI_{DSSP}} \]

\[ \tau = \frac{\tau_n + \tau_p}{2} = \frac{CV_{dd}}{4} \left[ \frac{1}{W_nI_{DSSN}} + \frac{1}{W_pI_{DSSP}} \right] \]

\[ \text{Pull-down} \]

\[ V_{in} \quad V_{out} \quad V_{dd} \]

\[ \text{Slope} = I_{NSAT}/C \]

\[ \tau_n \]

\[ \text{Pull-up} \]

\[ V_{in} \quad V_{out} \quad V_{dd} \]

\[ \text{Slope} = I_{PSAT}/C \]

\[ \tau_p \]
0.13 micron Cross Section (Copper)

Cu Interconnect 130nm Generation  Courtesy: IBM
90 nm Generation Interconnects

Source: Mark Bohr, Intel Corporation

Low-k CDO Dielectric

Copper Interconnects

7 layers of copper + new low-k CDO dielectric
65 nm Generation Interconnects

Cu Line
Cu Via
Low-k Carbon Doped Oxide

8 Cu interconnect layers for density and performance
Low-k CDO dielectric for performance and low power

Source: Mark Bohr, Intel Corporation
## Interconnect

![Interconnect Diagram](image)

### Interconnect Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Scaling Factor $(\kappa \geq 1)$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Interconnect dimensions $(t_w, L_w, W_w, t_{ins}, W_{sp})$</td>
<td>$1/\kappa$</td>
</tr>
<tr>
<td>Resistivity of conductor $(\rho_w)$</td>
<td>$1$</td>
</tr>
<tr>
<td>Insulator permittivity $(\varepsilon_{ins})$</td>
<td>$1$</td>
</tr>
<tr>
<td>Wire capacitance per unit length $(C_w)$</td>
<td>$1$</td>
</tr>
<tr>
<td>Wire resistance per unit length $(R_w)$</td>
<td>$\kappa^2$</td>
</tr>
<tr>
<td>Wire $RC$ delay $(\tau_w)$</td>
<td>$1$</td>
</tr>
<tr>
<td>Wire current density $(I / W_w t_w)$</td>
<td>$\kappa$</td>
</tr>
</tbody>
</table>

### Derived wire scaling behavior

- Assuming $K = 1/0.7 \sim 1.43$

  \[
  RC \text{ delay} = \left[ \frac{1}{0.7} \right]^2 \cdot R_w \cdot 0.7 \cdot C_w \cdot 0.7 = R_w C_w
  \]

  \[
  \frac{I}{W_w T_w} = \frac{0.7 \cdot I}{\left(0.7 \cdot W_w\right) \cdot \left(0.7 \cdot T_w\right)} = \frac{I}{0.7 \cdot W_w T_w}
  \]

---

An M4 5mm 0.18um line (1.8ns un-repeated) would scale to 3.5mm in 0.13um; assuming fF/um remains constant, but ohms/um doubles, then the same wire would take 3.6ns. Copper takes this to 1.0ns.
Repeated Interconnect

The 3.5mm M4 line’s 1ns can be further reduced to 0.52 ns by adding repeaters.

0.13 um Copper
# 90 nm & 65nm Technology Overview

<table>
<thead>
<tr>
<th></th>
<th>90 nm</th>
<th>65nm</th>
<th>units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lphysical</td>
<td>60/65</td>
<td>38/44</td>
<td>nm</td>
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<tr>
<td>Wmin</td>
<td>90</td>
<td>65</td>
<td>nm</td>
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<tr>
<td>Tox N/P</td>
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<td>1.4/1.4</td>
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<tr>
<td>Xj N/P</td>
<td>32/32</td>
<td>24/24</td>
<td>nm</td>
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<tr>
<td>CONTACT</td>
<td>90</td>
<td>65</td>
<td>nm</td>
</tr>
<tr>
<td>VIA1</td>
<td>130</td>
<td>95</td>
<td>nm</td>
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<tr>
<td>VIA2</td>
<td>130</td>
<td>95</td>
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<tr>
<td>VIA3</td>
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<td>VIA4</td>
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<td>175</td>
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<td>VIA5</td>
<td>240</td>
<td>175</td>
<td>nm</td>
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<tr>
<td>VIA6</td>
<td>340</td>
<td>300</td>
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</tr>
<tr>
<td>VIA7</td>
<td></td>
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<td>nm</td>
</tr>
<tr>
<td>POLY w/s</td>
<td>90/130</td>
<td>65/90</td>
<td>nm</td>
</tr>
<tr>
<td>M1 w/s</td>
<td>140/140</td>
<td>105/105</td>
<td>nm</td>
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<tr>
<td>M2 w/s</td>
<td>170/170</td>
<td>130/130</td>
<td>nm</td>
</tr>
<tr>
<td>M3 w/s</td>
<td>170/170</td>
<td>130/130</td>
<td>nm</td>
</tr>
<tr>
<td>M4 w/s</td>
<td>240/240</td>
<td>180/180</td>
<td>nm</td>
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<tr>
<td>M5 w/s</td>
<td>360/360</td>
<td>180/180</td>
<td>nm</td>
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<td>M6 w/s</td>
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<td>400/400</td>
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<tr>
<td>M7 w/s</td>
<td>810/810</td>
<td>400/400</td>
<td>nm</td>
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</table>
90 nm & 65nm Technology Overview –cnt’d–

<table>
<thead>
<tr>
<th></th>
<th>90 nm (Cu)</th>
<th>65nm</th>
<th>units</th>
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<tbody>
<tr>
<td>Vt0 N/P</td>
<td>0.3/-0.3</td>
<td>.29/-.33</td>
<td>volts</td>
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<tr>
<td>Rdsw N/P</td>
<td>300/600</td>
<td>378/748</td>
<td>ohms-um</td>
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<tr>
<td>Cj N/P</td>
<td>2.9/2.9</td>
<td>4.1/4.2</td>
<td>fF/um^2</td>
</tr>
<tr>
<td>Cjsw N/P</td>
<td>0.4/0.4</td>
<td>.34/.36</td>
<td>fF/um</td>
</tr>
<tr>
<td>Cgate N/P</td>
<td>~1.4</td>
<td>~1.8</td>
<td>fF/um</td>
</tr>
<tr>
<td>Idsat N/P</td>
<td>~1000/500</td>
<td>~1380/630</td>
<td>uA/um</td>
</tr>
<tr>
<td>Ioff N/P</td>
<td>60/-60</td>
<td>190/-175</td>
<td>nA/um @100C</td>
</tr>
</tbody>
</table>

|                     |            |          |         |
| CONTACT             | 4.0        | 8.0      | ohms/con @ 100C |
| VIA1                | 3.0        | 6.0      | ohms/con @ 100C |
| VIA2                | 2.4        | 6.0      | ohms/con @ 100C |
| VIA3                | 2.4        | 6.0      | ohms/con @ 100C |
| VIA4                | 1.4        | 4.5      | ohms/con @ 100C |
| VIA5                | 1.0        | 3.4      | ohms/con @ 100C |
| VIA6                | 0.6        | 2.0      | ohms/con @ 100C |
| VIA7                |            | 2.0      | ohms/con @ 100C |

|                     |            |          |         |
| M1 R & C            | 700 & 0.23 | 1570 & 0.23 | mohms/um & fF/um |
| M2 R & C            | 400 & 0.23 | 930 & 0.23  | mohms/um & fF/um |
| M3 R & C            | 400 & 0.23 | 930 & 0.22  | mohms/um & fF/um |
| M4 R & C            | 150 & 0.22 | 330 & 0.22  | mohms/um & fF/um |
| M5 R & C            | 150 & 0.23 | 330 & 0.23  | mohms/um & fF/um |
| M6 R & C            | 150 & 0.25 | 330 & 0.23  | mohms/um & fF/um |
| M7 R & C            | 100 & 0.25 | 100 & 0.25  | mohms/um & fF/um |
References

7. S. Thompson, et. al., 90nm Technology, 2002 IEDM Technical Digest, pp. 61-64.
8. P. Bai, et. al., “A 65nm Logic Technology Featuring 35nm Gate Length, Enhanced Channel Strain, 8 Cu Interconnect Layersw, Low-k ILD and 0.57um2 SRAM Cell”, 2004 IEDM.
9. Summary of a gazillion processors:
   http://www-vlsi.stanford.edu/group/chips_micropro.html
10. M. Bohr, Intel’s 90nm Process Starting High Volume Manufacturing,
    http://www.intel.com/research/silicon
11. For latest information on Intel’s silicon technology, please visit:
    http://www.intel.com/technology/silicon/
Drain Current Models

\[ I_{ds} = \mu_{eff} \frac{W}{L} \int_{0}^{V_{ds}} (-Q_i(v)) \, dv \]

\[ Q_i : \text{inversion charge per unit area} \]

Charge-sheet Approximation:

\[ I_{ds} = \mu_{eff} \, C_{ox} \frac{W}{L} \left[ (V_g - V_{fb} - 2\psi_B - \frac{V_{ds}}{2}) \, V_{ds} - \frac{2 \sqrt{\varepsilon_i q N_a}}{\varepsilon_{ox}} \left( (2 \psi_B + V_{ds})^{3/2} - (2 \psi_B)^{3/2} \right) \right] \]
Ids: Characteristics in the Linear Region

\[ I_{ds} = \mu_{\text{eff}} C_{ox} \frac{W}{L} \left( V_g - V_{fb} - 2 \psi_b - \frac{\sqrt{4 e_s q N_A \psi_b}}{C_{ox}} \right) V_{ds} \]

\[ = \mu_{\text{eff}} C_{ox} \frac{W}{L} \left( V_g - V_T \right) V_{ds} \]

\[ 2 \psi_b = \frac{2 kT}{q} \ln \left( \frac{N_a}{n_i} \right) \]
Ids: Characteristics in the Subthreshold Region

\[-Q_i = \sqrt{\frac{\varepsilon_{Si} q N_A}{2 \psi_s}} \left( \frac{kT}{q} \right) \left( \frac{\kappa_i}{N_A} \right)^2 \leq \frac{q (\psi_b - V)/kT}{1 - \frac{V_{ds}}{kT}}\]

\[I_{ds} = \mu_{eff} \frac{W}{L} \sqrt{\frac{\varepsilon_{Si} q N_A}{4 \psi_s}} \left( \frac{kT}{q} \right)^2 \leq \frac{4(V_g - V_T) m kT}{1 - \frac{V_{ds}}{kT}}\]

\[m = 1 + \frac{C_{dw}}{C_{ox}} \sim 1 + \frac{3 \varepsilon_{ox}}{W d_m}\]

\[S = \left( \frac{d \log_{10}(I_{ds})}{dV_g} \right)^{-1} = 2.3 \frac{m kT}{q}\]

Characteristics in the Saturation Region (Long Channel)

\[ I_{ds} = \mu_{eff} C_{ox} \frac{W}{L} \left[ (V_g - V_T) V_{ds} - \frac{m}{2} V_{ds}^2 \right] \]

at \( V_{dsat} = \frac{V_g - V_T}{m} \) and \( m = 1 + \frac{C_{dm}}{C_{ox}} \)

\[ I_{dsat} = \mu_{eff} C_{ox} \frac{W}{L} (V_g - V_T)^2 \cdot \frac{1}{2m} \]

Characteristics in the Saturation Region with Velocity Saturation

\[ V = \frac{\mu_{\text{eff}} E}{\left[ 1 + \left( \frac{E}{E_c} \right)^n \right]^{1/n}} \quad \text{n=2 electrons} \]
\[ V_{\text{sat}} = \mu_{\text{eff}} E_c \]

For \( n=0 \) (PFETs):

\[ I_{ds} = \frac{-\mu_{\text{eff}} W}{L} \int V_{ds} Q_i(V) dV \]

Long channel current

\[ I_{ds} = \frac{C_{ox} W V_{\text{sat}} (V_g - V_T) \sqrt{1 + 2/\mu_{\text{eff}} (V_g - V_T)/\mu_{s\text{sat}} L} - 1}{\sqrt{1 + 2/\mu_{\text{eff}} (V_g - V_T)/\mu_{s\text{sat}} L} + 1} \]

\[ \text{if} \quad \frac{V_{ds}}{L} \ll V_{\text{sat}} \]
Characteristics in the Saturation Region with Velocity Saturation

Interconnect Delay

- Delay without the wire:
  \[ \text{Delay} = R_{\text{trans}} C_{\text{load}} \]
- Added delay from wire:
  The intrinsic wire delay \( \frac{1}{2} R_W C \)
  Added delay from the wire cap \( R_{\text{trans}} C \)
  Added delay from the wire resistance \( R_W C_{\text{load}} \)
  \[ \text{Delay} = R_{\text{trans}}(C+C_{\text{load}}) + R_W(C/2+C_{\text{load}}) \]

\[ \text{Intrinsic wire delay} \approx 0.5L^2(R/\mu\text{m})(C/\mu\text{m}) \]
Wire Delay Example

- In 0.18 um CMOS, assume a 2 mm M2 wire, minimum width (0.34um), and a 120fF load at the end.

- What is the intrinsic wire delay?
- What size driver should you use?

- Intrinsic Delay:
  - Using a worst case 0.18 ohms/um and 0.22 fF/um:  
  - \( C = 2000 \times 0.22 = 440 \) fF and \( R = 360 \) ohms.  
  - Intrinsic wire delay = 0.5*RC ~ 79ps

- Driver size (use FO=4 and P:N ratio~2):
  - input cap ~ (Cwire+Cload)/4 ~ \( \frac{560fF}{4} = 140fF \)
  - Using Cox ~1fF/um, PFET is 93um and NFET is 47um.

- If M2 wire is 4mm long, intrinsic delay is ~ 317ps ...... 4X longer ....
Homework Assignment #1.2 & #1.4

A 2 cycle static circuit will be analyzed with a Copper 1.0V, 90nm CMOS technology. Maximum frequency (Fmax) of operation and power dissipation as a function of VDD with ZERO clock skew will be established via circuit simulation. In addition, the impact of realistic clock skew on Fmax will be determined. Finally, the Fmax will be predicted for a 65nm CMOS circuit using constant field scaling law.
All dimensions in microns
90nm CMOS
R in ohms, C in fF
Clock-Skew Impact to Fmax (HMK #1.4)

\[ \tau_1 > \tau_2 \]
INVERTING MSFF