Labs - 30% V
Ex 1 - 15%
Ex 2 - 7
Programming (Timed)

- Tue (Office hrs)
- checkout - Wed @ 2-4
- TA: Explain Thu
- scan: Next lab
Embedded Systems

Sensors
- Actuators
- Outputs
- Temperature
- Distance
- Sliders/tools

Architecture - Von Neumann Arch

ARM

Havard Architecture (Multiple Buses)

Data Bus

Instruction Bus

I/O Bus

Bus

ROM

RAM

CPU
ARM ISA
- Instruction set 200+ x86 LC3
- Registers - 16
- Addressing Modes
- Memory Layout

LDR  ADD  STR
RO, Count  RO, RO, #1  RO, count

count = count + 1;

Load-Store Arch

LDR  RO, [R1]
LDR  R5, #1

CPU ALU

RAM

Register

count 5

SP
LR
PC
LR  R12
R13  R14
R15
ARM
Memory Layout

Register

32 bits

2x20000-FFFF

256KB ROM

8-bit

TM4C

Instruction
Constants

Data

MAR

2x4000-FFFF

MDR

2x4FFFF-FFFF

JSR 16+32 bits

0x0000-FFFF

J/IO

Internal I/O

32KB RAM
Port access

Init
1. Turn on clock for Port
2. Wait to stabilize
3. DEN
4. DIR
5. AFSEL (Alt function)

Access

DATA