Final Exam Solutions

Date: May 14, 2015

UT EID: ___________________  Circle one: MT, NT, JV, RY, VJR

Printed Name: ___________________  ___________________
                       Last,                   First

Your signature is your promise that you have not cheated and will not cheat on this exam, nor will you help others to cheat on this exam. *You will not reveal the contents of this exam to others who are taking the makeup thereby giving them an undue advantage*:

Signature: __________________________________________

Instructions:

• Closed book and closed notes. No books, no papers, no data sheets (other than the last four pages of this Exam)
• No devices other than pencil, pen, eraser (no calculators, no electronic devices), please turn cell phones off.
• Please be sure that your answers to all questions (and all supporting work that is required) are contained in the space (boxes) provided. *Anything outside the boxes will be ignored in grading*.
• You have 180 minutes, so allocate your time accordingly.
• For all questions, unless otherwise stated, find the most efficient (time, resources) solution.
• Unless otherwise stated, make all I/O accesses friendly.
• *Please read the entire exam before starting. See supplement pages for Device I/O registers*.

<table>
<thead>
<tr>
<th>Problem</th>
<th>Score</th>
</tr>
</thead>
<tbody>
<tr>
<td>Problem 1</td>
<td>10</td>
</tr>
<tr>
<td>Problem 2</td>
<td>10</td>
</tr>
<tr>
<td>Problem 3</td>
<td>10</td>
</tr>
<tr>
<td>Problem 4</td>
<td>10</td>
</tr>
<tr>
<td>Problem 5</td>
<td>10</td>
</tr>
<tr>
<td>Problem 6</td>
<td>10</td>
</tr>
<tr>
<td>Problem 7</td>
<td>12</td>
</tr>
<tr>
<td>Problem 8</td>
<td>8</td>
</tr>
<tr>
<td>Problem 9</td>
<td>20</td>
</tr>
<tr>
<td>Total</td>
<td>100</td>
</tr>
</tbody>
</table>
(10) Question 1. Please place one letter/number for each box. Choose the best answer to each question.

Part i) Why do we sometimes use the phase lock loop? .................. Y

Part ii) Why did we use the open collector 7406 gate to interface the LED? .................. M

Part iii) Why did we use fixed-point to represent measured distance? .................. G

Part iv) Why did we dump input/output data into buffers in Lab 4? .................. J

Part v) Why do we put programs in flash memory? .................. I

Part vi) Why does the UART use start and stop bits? .................. T

Part vii) Why do we specify a global variable as static? .................. D

Part viii) Why do we specify a local variable as static? .................. Z

Part ix) Why do the I/O definitions have volatile in the definitions? .................. X

Part x) Why do we specify a function parameter as const? .................. V

A) The Cortex M has a Harvard Architecture.
B) The PC always fetches instructions from flash memory in a von Neumann architecture.
C) Some machine instructions are 16 bits and others are 32 bits.
D) It reduces the scope of the data making the data private to the file.
E) The Cortex M processor on the TM4C123 does not support floating point operations.
F) The left/right shift is faster than multiply/divide.
G) In order to represent non-integer values.
H) To create bounded latency and provide for real-time operation.
I) It is nonintrusive debugging.
J) It is minimally intrusive debugging.
K) The interface must control both voltage and current so the LED is the proper brightness.
L) The LED needs more than 3.3 V.
M) The LED needs more than 8 mA.
N) Buffers can store more data than can be printed using the UART.
O) It creates a negative logic interface.
P) To satisfy the Nyquist Theorem.
Q) It illustrates to our client how the program works.
R) Because the UART sends a data bit value 0 as 0V and a data bit value 1 at 3.3V.
S) Message can vary in length and it is used signify the end of the message.
T) The receiver uses it to synchronize timing with the transmitter.
U) It provides a mechanism to minimize bandwidth.
V) Black box testing is more detailed than white box testing.
W) It decouples the production of data from the consumption of data.
X) It provides for ceiling and floor.
Y) If we slow down processor execution, it will save power. If we execute faster, we do more processing.
Z) It provides for debugging, allowing you to download code and debug your software.

1) In order to handle either positive or negative values.
2) To allocate it in RAM, making it persistent across subroutine calls.
3) To allocate it in ROM, and ROM is nonvolatile.
4) To tell the compiler to fetch a new value each time it is accessed.
5) To tell the compiler the subroutine should not change its value.
6) Specifies it as an address or a pointer.
(10) Question 2

(2) Part a) What are the addressing modes used in the following ARM instructions?

<table>
<thead>
<tr>
<th>Instructions</th>
<th>Addressing Modes</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOV R0, #10</td>
<td>Immediate mode</td>
</tr>
<tr>
<td>LDR R0, [R1]</td>
<td>Indexed addressing</td>
</tr>
<tr>
<td>BL sublabel</td>
<td>PC-relative</td>
</tr>
<tr>
<td>ADD R2, R1</td>
<td>Register</td>
</tr>
<tr>
<td>PUSH {R4-R11, LR}</td>
<td>Register list</td>
</tr>
</tbody>
</table>

(2) Part b) In order to specify the desired baud rate for a bus clock frequency is 80 MHz, the divider has been correctly calculated as 50.125. What values should the UART0_IBRD_R and the UART0_FBRD_R registers be initialized to?

\[
\text{UART0_IBRD}_R = 50 \\
\text{UART0_FBRD}_R = 8
\]

(2) Part c) If the ADC sampling frequency is 100 Hz, what range of frequencies in the analog input can safely be represented in the digital samples?

Nyquist Theorem, 0 to 50 Hz

(2) Part d) Consider an LED with a desired operating point of \((I_d, V_d)\). Let \(V_{OL}, V_{OH}\), \(I_{OL}\) and \(I_{OH}\) be the operating parameters of the digital output on PA1. What is the design equation needed to calculate the desired resistance \(R\) for this circuit?

\[
R = \frac{(3.3 - V_d - V_{OL})}{I_d}
\]

(2) Part e) What is the relationship between the range, precision and resolution of an ADC, given that the sampling frequency is \(f\)?

Range = precision * resolution
Question 3. Reverse-engineer UART parameters from the trace observed at a receiver below.

(2) Part a) What is the data value transferred over the UART in hexadecimal?

(1) Part b) What is the baud rate in bits/sec?

(2) Part c) What is the maximum bandwidth in bytes per second?

(3) Part d) Assume the UART has been initialized with busy wait synchronization. Write a C function that reads one character from the UART.

```c
char UART_Read(void){
    while((UART0_FR_R & 0x0010) == 0); // RXFE
    return ((char)(UART0_DR_R & 0xFF));
}
```

(2) Part e) Assume the receiver software uses busy-wait synchronization. The main program reads all the data available from the UART and then processes the data. The maximum time required to process the data is 125us. Is it possible to lose data? If so, explain how to change the UART so no data is lost. If no data can be lost, explain how the UART works so no data are lost.

Add FIFOs for rate matching. At least 3 bytes. The TM4C123 will not lose data because it has a 16-element FIFO.
(10) **Question 4.** Analog Devices AD7641 is an 18-bit, 0 to 2.5V range, 2MSPS SAR ADC. A student is attempting to capture a sinusoid signal of frequency 7.5 kHz using the AD7641. Using the 18-bit ADC and periodic interrupt, he programs the system to interrupt at a frequency of 20 kHz. Each time the system interrupts, he calls `AD7641_In()` to get one sample of the signal from the AD7641.

(2) **Part a)** If the AD7641 input is 1.25 V, what will be the digital value in hex returned by this ADC?

\[ 2^{17} = 0 \times 20000 \]

(4) **Part b)** Assuming the first sample is taken at time \( t = 0 \), mark the (time, voltage) points on the plot below specifying the data collected by the ADC. **Red dots are the digital samples**

![Plot of sinusoid signal](image)

(4) **Part c)** Is it possible to recreate the original signal from the captured samples? If your answer is yes, explain how. If your answer is no, what is the term used to refer to this loss of information?

Yes, it is possible because 7.5 kHz is less than \( \frac{1}{2} f_s \) according to the Nyquist Theorem
**Question 5.** You will design an embedded system using a Moore FSM. There are two inputs (PB3, PB2) and two outputs (PB1, PB0). The FSM runs in the background with 1 kHz SysTick periodic interrupts. Initially both outputs will be low, and you may also assume both inputs are initially low. If PB3 rises before PB2 rises, then set PB1 high. If PB2 rises before PB3 rises, then set PB0 high. If both rise during the same 1-ms window, set both PB1 and PB0 high. After either or both PB1 and/or PB0 become high, let the output remain fixed. The initial state is s=0.

**Part a)** Show the FSM graph in Moore format. Full credit for the solution with the fewest states.

![FSM Diagram](image)

**Part b)** The `struct` and the main program are fixed. Show the C code that places the FSM in ROM, and write the SysTick ISR. `PORTB_Init` initializes PB3-PB0 and makes the outputs low. `SysTick_Init` initializes interrupts at 1 kHz. `PORTB_Init` and `SysTick_Init` are given. Full credit awarded for friendly access and good programming style. The initial state will be s=0.

```c
const struct State{
    uint32_t out;
    uint32_t next[4];
};
typedef const struct State State_t;
uint32_t s;  // state number

void main(void){
    PORTB_Init();
    s = 0; // initial state
    SysTick_Init();
    EnableInterrupts();
    while(1){
        // Initialize array of states
        #define Check 0
        #define PB2 1
        #define PB3 2
        #define Both 3
        State_t FSM[4]={
            {0, {Check, PB2, PB3, Both}},
            {1, {PB2, PB2, PB2, PB2}},
            {2, {PB3, PB3, PB3, PB3}},
            {3, {Both, Both, Both, Both}}};

        // read input
        in = GPIO_PORTB_DATA_R&0x0C>>2;

        // change state
        s = FSM[s].next[in];

        // friendly write output
        out = GPIO_PORTB_DATA_R&(~0x03);
        out |= FSM[s].out;
        GPIO_PORTB_DATA_R = out;
    }
}
```
(10) Question 6. (a): You are given two 1 kΩ resistors and four 2 kΩ resistors. Build a 3-bit DAC circuit (connected to PE2, PE1, PE0) using *all* resistors. Complete the table below where a few of the input logic voltage values at PE2, PE1, PE0 are shown. Calculate the output voltage \( V_{\text{out}} \) of the DAC for those input values given that \( V_{\text{OH}} = 5.0 \text{V} \), and \( V_{\text{OL}} = 0 \text{V} \)

<table>
<thead>
<tr>
<th>PE2</th>
<th>PE1</th>
<th>PE0</th>
<th>( V_{\text{out}} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0 V</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0.625 V</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1.25 V</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>2.5 V</td>
</tr>
</tbody>
</table>

(b) The output of the DAC circuit you built in part (a) is now connected to a speaker whose resistance is very low and can be approximated to be 0 Ω. Calculate the current through the speaker when the logic voltage values at PE2, PE1, PE0 are 100. Show your work

For the R-2R ladder circuit:
Current = \( 5/2k = 2.5 \text{ mA} \)

For the weighted DAC circuit:
Current = \( 5/1k = 5 \text{ mA} \)
(12) Question 7: FIFO
(2) Part a) What is the difference between FIFO and Mailbox?

Mailbox holds one piece of data, while a FIFO can hold multiple data in a first in first out manner.

(10) Part b) Write a C program that implements FIFO using two stack data structures. You have to implement the \texttt{Fifo\_Get} function using two stacks. \texttt{Fifo\_Put} is already given to you. Return a value of -1 if the FIFO is empty. The stack data functions are given to you, having \textit{push, pop and empty} functions that you must use. The function prototypes for these functions are given below.

// Prototypes of the stack functions that you can use
// Assume stacks do not overflow (infinite size)
int pop1(); // Gets the element at the top of the stack1
void push1(int); // Puts the element at the top of the stack1
int empty1(); // Returns 1 if stack1 is empty, 0 otherwise
int pop2(); // Gets the element at the top of the stack2
void push2(int); // Puts the element at the top of the stack2
int empty2(); // Returns 1 if stack2 is empty, 0 otherwise

// Put an element into the back of the FIFO.
// data is never -1 (the error code)
void Fifo\_Put(int data) {
    push1(data); // pushes element data onto stack1
}

// Get the element at the head of the FIFO
int Fifo\_Get(void) {
    int value;
    if (!empty2()) {
        return pop2();
    }

    while (!empty1()) {
        value = pop1();
        push2(value);
    }

    if (!empty2()) {
        return pop2();
    }
    return -1;
}
(8) **Question 8**: Convert the C code into assembly, using local variable allocation phases. Remember, local variables use the stack, not registers. Put exactly one assembly line into each box.

```assembly
; *****binding phase**************
.sum EQU 0 ;16-bit unsigned number
.n EQU 2 ;16-bit unsigned number

; 1)*****allocation phase *********
calc PUSH {R4,LR}
    SUB SP,#4 ;allocate 4 bytes

; 2)******access phase ************
    MOV R0,#0
    STRH R0,[SP,#sum] ;sum=0

    MOV R1,#255
    STRH R1,[SP,#n] ;n=255

    loop LDRH R1,[SP,#n] ;R1=n
        LDRH R0,[SP,#sum] ;R0=sum
        ADD R0,R1 ;R0=sum+n
        STRH R0,[SP,#sum] ;sum=sum+n
    LDRH R1,[SP,#n] ;R1=n
    SUBS R1,#1 ;n-1
    STRH R1,[SP,#n] ;n=n-1

    BNE loop ; 3)*****deallocation phase *****

    ADD SP,#4 ;deallocation
    POP {R4,PC} ;R0=sum
```

```c
uint16_t calc(void){
    uint16_t sum;
    uint16_t n;
    sum = 0;
    for(n=255; n>0; n--){
        sum = sum + n;
    }
    return sum;
}
```
(20) Question 9: (Program) Many of you could not play your ideal music for Lab 10. Valvano had enough with people asking for Full licenses on Keil, he knows sound files are the source of the problem, they are simply too big. You are told to change the coding of the sound files so the resulting array packs two 4-bit samples into one byte, resulting in a compression ratio of 2:1. All wav files are converted to 4-bit samples at 8 kHz. For example the first ten 4-bit samples of the start sound (see below) are 8,9,9,10,11,11,12,14,15,15. Notice 8,9 are “packed” into the byte 0x89. During play time, the packed values are decompressed into their original form and sent to the DAC. The game has 4 sounds, each in a different array named startS, shootS, deathS and quietS, each of a different length. The following code declares the constants, variables and structure used in the solution. Read the code carefully and answer the below questions.

```
#define start 0
#define shoot 1
#define death 2
#define quiet 3

const uint8_t startS[450] = {0x89,0x9A,0xBB,0xCE,0xFF … };  
const uint8_t shootS[280] = { … };  
const uint8_t deathS[8]   = {0x8B,0xDE,0xFE,0xDB,0x85,0x32,0x12,0x35};  
const uint8_t quietS[1]   = {0x88};
struct sound{
    uint32_t length;     // number of bytes in the array
    const uint8_t *samples;  // pointer to the array
};
typedef struct sound Sound_t;

// sounds is the array of structs one per sound
Sound_t sounds[4] = {{450,startS},{280,shootS},{8,deathS},{1,quietS}};

uint32_t cSound; // holds the current sound number (0,1,2,or 3)
```

Your task is to write the following three routines, along with any globals you need above:

```
// Setup SysTick so it interrupts periodically at 8 kHz, bus=80MHz
void SysTick_Init(void){
    NVIC_ST_CTRL_R = 0;
    NVIC_ST_RELOAD_R = 9999; // 80MHz/8kHz = 10000
    NVIC_ST_CURRENT_R = 0;
    cSound = quietS; Index = 0; hi = 1;

    NVIC_SYS_PRI3_R = (NVIC_SYS_PRI3_R&0x00FFFFFF)|0x40000000;// Priority 2
    NVIC_ST_CTRL_R = 0x07; // CS=1, IEN=1, EN=1
}
```
void ChangeSound(uint8_t soundNum) {
    cSound = soundNum;
    Index = 0;
    NVIC_ST_CURRENT_R = 0;
    hi = 1;
}

void SysTickHandler(void) {
    if(hi){
        DAC_Out((sounds[cSound].samples[Index]>>4);
        hi = 0;
    }else{
        DAC_Out(sounds[cSound].samples[Index]&0x0F);
        hi = 1;
        Index++; // increment every other output
    }
    if(Index==sounds[cSound].length){
        Index = 0;
    }
}
Memory access instructions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>LDR Rd, [Rn]</td>
<td>load 32-bit number at [Rn] to Rd</td>
</tr>
<tr>
<td>LDR Rd, [Rn,#off]</td>
<td>load 32-bit number at [Rn+off] to Rd</td>
</tr>
<tr>
<td>LDR Rd, =value</td>
<td>load unsigned 16-bit at [Rn] to Rd</td>
</tr>
<tr>
<td>LDRH Rd, [Rn]</td>
<td>load signed 16-bit at [Rn] to Rd</td>
</tr>
<tr>
<td>LDRH Rd, [Rn,#off]</td>
<td>load signed 16-bit at [Rn+off] to Rd</td>
</tr>
<tr>
<td>LDRB Rd, [Rn]</td>
<td>load unsigned 8-bit at [Rn] to Rd</td>
</tr>
<tr>
<td>LDRB Rd, [Rn,#off]</td>
<td>load unsigned 8-bit at [Rn+off] to Rd</td>
</tr>
<tr>
<td>LDRB Rd, [Rn]</td>
<td>load signed 8-bit at [Rn] to Rd</td>
</tr>
<tr>
<td>LDRB Rd, [Rn,#off]</td>
<td>load signed 8-bit at [Rn+off] to Rd</td>
</tr>
<tr>
<td>STR Rt, [Rn]</td>
<td>store 32-bit Rt to [Rn]</td>
</tr>
<tr>
<td>STR Rt, [Rn,#off]</td>
<td>store 32-bit Rt to [Rn+off]</td>
</tr>
<tr>
<td>STRH Rt, [Rn]</td>
<td>store least sig. 16-bit Rt to [Rn]</td>
</tr>
<tr>
<td>STRH Rt, [Rn,#off]</td>
<td>store least sig. 16-bit Rt to [Rn+off]</td>
</tr>
<tr>
<td>STRB Rt, [Rn]</td>
<td>store least sig. 8-bit Rt to [Rn]</td>
</tr>
<tr>
<td>STRB Rt, [Rn,#off]</td>
<td>store least sig. 8-bit Rt to [Rn+off]</td>
</tr>
<tr>
<td>PUSH {Rt}</td>
<td>push 32-bit Rt onto stack</td>
</tr>
<tr>
<td>POP {Rd}</td>
<td>pop 32-bit number from stack into Rd</td>
</tr>
<tr>
<td>ADR Rd, label</td>
<td>set Rd equal to the address at label</td>
</tr>
<tr>
<td>MOV{S} Rd, &lt;op2&gt;</td>
<td>set Rd equal to op2</td>
</tr>
<tr>
<td>MOV Rd, #im16</td>
<td>set Rd equal to im16, im16 is 0 to 65535</td>
</tr>
<tr>
<td>MVN{S} Rd, &lt;op2&gt;</td>
<td>set Rd equal to -op2</td>
</tr>
</tbody>
</table>

Branch instructions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>B label</td>
<td>branch to label Always</td>
</tr>
<tr>
<td>BEQ label</td>
<td>branch if Z == 1 Equal</td>
</tr>
<tr>
<td>BNE label</td>
<td>branch if Z == 0 Not equal</td>
</tr>
<tr>
<td>BCS label</td>
<td>branch if C == 1 Higher or same, unsigned ≥</td>
</tr>
<tr>
<td>BHS label</td>
<td>branch if C == 1 Higher or same, unsigned ≥</td>
</tr>
<tr>
<td>BCC label</td>
<td>branch if C == 0 Lower, unsigned &lt;</td>
</tr>
<tr>
<td>BLO label</td>
<td>branch if C == 0 Lower, unsigned &lt;</td>
</tr>
<tr>
<td>BMI label</td>
<td>branch if N == 1 Negative</td>
</tr>
<tr>
<td>BPL label</td>
<td>branch if N == 0 Positive or zero</td>
</tr>
<tr>
<td>BVS label</td>
<td>branch if V == 1 Overflow</td>
</tr>
<tr>
<td>BVC label</td>
<td>branch if V == 0 No overflow</td>
</tr>
<tr>
<td>BHI label</td>
<td>branch if C==1 and Z==0 Higher, unsigned &gt;</td>
</tr>
<tr>
<td>BLS label</td>
<td>branch if C==0 or Z==1 Lower or same, unsigned ≤</td>
</tr>
<tr>
<td>BGE label</td>
<td>branch if N == V Greater than or equal, signed ≥</td>
</tr>
<tr>
<td>BLT label</td>
<td>branch if N != V Less than, signed &lt;</td>
</tr>
<tr>
<td>BGT label</td>
<td>branch if Z==0 and N==V Greater than, signed &gt;</td>
</tr>
<tr>
<td>BLE label</td>
<td>branch if Z==1 or N!=V Less than or equal, signed ≤</td>
</tr>
<tr>
<td>BX Rm</td>
<td>branch indirect to location specified by Rm</td>
</tr>
<tr>
<td>BL label</td>
<td>branch to subroutine at label</td>
</tr>
<tr>
<td>BLX Rm</td>
<td>branch to subroutine indirect specified by Rm</td>
</tr>
</tbody>
</table>

Interrupt instructions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPSIE I</td>
<td>enable interrupts (I=0)</td>
</tr>
<tr>
<td>CPSID I</td>
<td>disable interrupts (I=1)</td>
</tr>
</tbody>
</table>

Logical instructions

<table>
<thead>
<tr>
<th>Instruction</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>AND{S} {Rd,} Rn, &lt;op2&gt;</td>
<td>Rd=Rn&amp;op2 (op2 is 32 bits)</td>
</tr>
<tr>
<td>ORR{S} {Rd,} Rn, &lt;op2&gt;</td>
<td>Rd=Rn</td>
</tr>
<tr>
<td>EOR{S} {Rd,} Rn, &lt;op2&gt;</td>
<td>Rd=Rn^op2 (op2 is 32 bits)</td>
</tr>
<tr>
<td>BIC{S} {Rd,} Rn, &lt;op2&gt;</td>
<td>Rd=Rn&amp;(~op2) (op2 is 32 bits)</td>
</tr>
<tr>
<td>ORN{S} {Rd,} Rn, &lt;op2&gt;</td>
<td>Rd=Rn</td>
</tr>
<tr>
<td>LSR{S} Rd, Rm, Rs</td>
<td>logical shift right Rd=Rm&gt;&gt;Rs (unsigned)</td>
</tr>
<tr>
<td>LSR{S} Rd, Rm, #n</td>
<td>logical shift right Rd=Rm&gt;&gt;n (unsigned)</td>
</tr>
<tr>
<td>ASR{S} Rd, Rm, Rs</td>
<td>arithmetic shift right Rd=Rm&gt;&gt;Rs (signed)</td>
</tr>
</tbody>
</table>
ASR(S) Rd, Rm, #n ; arithmetic shift right Rd=Rm>>n (signed)
LSL(S) Rd, Rm, Rs ; shift left Rd=Rm<<Rs (signed, unsigned)
LSL(S) Rd, Rm, #n ; shift left Rd=Rm<<n (signed, unsigned)

Arithmetic instructions
ADD(S) {Rd,} Rn, <op2> ; Rd = Rn + op2
ADD(S) {Rd,} Rn, #im12 ; Rd = Rn + im12, im12 is 0 to 4095
SUB(S) {Rd,} Rn, <op2> ; Rd = Rn - op2
SUB(S) {Rd,} Rn, #im12 ; Rd = Rn - im12, im12 is 0 to 4095
RSB(S) {Rd,} Rn, <op2> ; Rd = op2 - Rn
RSB(S) {Rd,} Rn, #im12 ; Rd = im12 – Rn
CMP Rn, <op2> ; Rn – op2 sets the NZVC bits
CMN Rn, <op2> ; Rn - (-op2) sets the NZVC bits
MUL(S) {Rd,} Rn, Rm ; Rd = Rn * Rm signed or unsigned
MLA Rd, Rn, Rm, Ra ; Rd = Ra + Rn*Rm signed or unsigned
MLS Rd, Rn, Rm, Ra ; Rd = Ra - Rn*Rm signed or unsigned
UDIV {Rd,} Rn, Rm ; Rd = Rn/Rm unsigned
SDIV {Rd,} Rn, Rm ; Rd = Rn/Rm signed

Notes
Ra Rd Rm Rn Rt represent 32-bit registers
value any 32-bit value: signed, unsigned, or address
{S} if S is present, instruction will set condition codes
#im12 any value from 0 to 4095
#im16 any value from 0 to 65535
{Rd,} if Rd is present Rd is destination, otherwise Rn
#n any value from 0 to 31
#off any value from -255 to 4095
label any address within the ROM of the microcontroller
op2 the value generated by <op2>

Examples of flexible operand <op2> creating the 32-bit number. E.g., Rd = Rn+op2
ADD Rd, Rn, Rm ; op2 = Rm
ADD Rd, Rn, Rm, LSL #n ; op2 = Rm<<n Rm is signed, unsigned
ADD Rd, Rn, Rm, LSR #n ; op2 = Rm>>n Rm is unsigned
ADD Rd, Rn, Rm, ASR #n ; op2 = Rm>>n Rm is signed
ADD Rd, Rn, #constant ; op2 = constant, where X and Y are hexadecimal digits:
• produced by shifting an 8-bit unsigned value left by any number of bits
• in the form 0x00XY00XY
• in the form 0xXY00XY00
• in the form 0xXYXYXYXY

General purpose registers

Stack pointer
Link register
Program counter

Condition code bits
N negative
Z zero
V signed overflow
C carry or unsigned overflow

256k Flash ROM 0x0000.0000
64k RAM 0x0003.FFFF
I/O ports 0x2000.0000
Internal I/O PPB 0x2000.FFFF

DCB 1,2,3 ; allocates three 8-bit byte(s)
DCW 1,2,3 ; allocates three 16-bit halfwords
DCD 1,2,3 ; allocates three 32-bit words
SPACE 4 ; reserves 4 bytes
When using sequencer 3, there is only one sample, so TM4C123/LM4F120. Which channel we sample is configured by writing to the ADC_SSCTL3_R
IE0 for both interrupt and busy-wait synchronization. ADC conversion, and clear it when no flags are needed. We will set conversion is complete. We can enable and disable the sequencers using the ADC_EMUX_R to specify how the ADC will be triggered. If we specify software start (EM3), then the software writes an 8 (SS3) to the ADC_PSSI_R to initiate a conversion on sequencer 3. Bit 3 (INR3) in the ADC_RIS_R register will be set when the conversion is complete. We can enable and disable the sequencers using the ADC_ACTSS_R register. There are 11 on the TM4C123/LM4F120. Which channel we sample is configured by writing to the ADC_SSMUX3_R register. The ADC_SSSCTL3_R register specifies the mode of the ADC sample. Clear TS0. We set IE0 so that the INR3 bit is set on ADC conversion, and clear it when no flags are needed. We will set IE0 for both interrupt and busy-wait synchronization.

Table 4.5. Some TM4C123/LM4F120 parallel ports. Each register is 32 bits wide. Bits 31 – 8 are zero.

<table>
<thead>
<tr>
<th>Address</th>
<th>31</th>
<th>30</th>
<th>29-7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>$0xE000E100</td>
<td>F</td>
<td>...</td>
<td>UART1</td>
<td>UART0</td>
<td>E</td>
<td>D</td>
<td>C</td>
<td>B</td>
<td>A</td>
<td>NVIC_EN0_R</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Address</th>
<th>31-24</th>
<th>23-17</th>
<th>16</th>
<th>15-3</th>
<th>2</th>
<th>1</th>
<th>0</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>$E000E010</td>
<td>0</td>
<td>0</td>
<td>COUNT</td>
<td>0</td>
<td>CLK_SRC</td>
<td>INTEN</td>
<td>ENABLE</td>
<td>NVIC_ST_CTRL_R</td>
</tr>
<tr>
<td>$E000E014</td>
<td>0</td>
<td>24-bit RELOAD value</td>
<td>NVIC_ST_RELOAD_R</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$E000E018</td>
<td>0</td>
<td>24-bit CURRENT value of SysTick counter</td>
<td>NVIC_ST_CURRENT_R</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 9.6 shows the SysTick registers used to create a periodic interrupt. SysTick has a 24-bit counter that decrements at the bus clock frequency. Let $f_{bus}$ be the frequency of the bus clock, and let $n$ be the value of the RELOAD register. The frequency of the periodic interrupt will be $f_{bus}/(n+1)$. First, we clear the ENABLE bit to turn off SysTick during initialization. Second, we set the RELOAD register. Third, we write to the NVIC_ST_CURRENT_R value to clear the counter. Lastly, we write the desired mode to the control register, NVIC_ST_CTRL_R. To turn on the SysTick, we set the ENABLE bit. We must set CLK_SRC=1, because CLK_SRC=0 external clock mode is not implemented on the LM3S/LM4F family. We set INTEN to enable interrupts. The standard name for the SysTick ISR is SysTick_Handler.

<table>
<thead>
<tr>
<th>Address</th>
<th>31-17</th>
<th>16</th>
<th>15-10</th>
<th>9</th>
<th>8</th>
<th>7-0</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td>$0xE00F.E000</td>
<td>ADC</td>
<td>MAXADCS PD</td>
<td>SYSTICK RCGC0 R</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$0x400E.8020</td>
<td>SS3</td>
<td>SS2</td>
<td>SS1</td>
<td>SS0</td>
<td>ADC_SSPRI_R</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>15-12</td>
<td>11-8</td>
<td>7-4</td>
<td>3-0</td>
<td>ADC_EMUX_R</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$0x400E.8014</td>
<td>EM3</td>
<td>EM2</td>
<td>EM1</td>
<td>EM0</td>
<td>ADC_EMUX_R</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$0x400E.8000</td>
<td>ASEN3</td>
<td>ASEN2</td>
<td>ASEN1</td>
<td>ASEN0</td>
<td>ADC_ACTSS_R</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$0x400E.80A0</td>
<td>MUX0</td>
<td>ADC_SSMUX3 R</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$0x400E.80A4</td>
<td>TS0</td>
<td>IE0</td>
<td>END0</td>
<td>D0</td>
<td>ADC_SSSCTL3_R</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$0x400E.8028</td>
<td>SS3</td>
<td>SS2</td>
<td>SS1</td>
<td>SS0</td>
<td>ADC_PSSI_R</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$0x400E.8004</td>
<td>INR3</td>
<td>INR2</td>
<td>INR1</td>
<td>INR0</td>
<td>ADC_RIS_R</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$0x400E.8008</td>
<td>MASK3</td>
<td>MASK2</td>
<td>MASK1</td>
<td>MASK0</td>
<td>ADC_IM_R</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$0x400E.800C</td>
<td>IN3</td>
<td>IN2</td>
<td>IN1</td>
<td>IN0</td>
<td>ADC ISC_R</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Table 9.6. SysTick registers.

Table 10.3. The TM4C123/LM4F120ADC registers. Each register is 32 bits wide. Set MAXADCS PD to 00 for slow speed operation. The ADC has four sequencers, but we will use only sequencer 3. We set the ADC_SSPRI_R register to 0x3210 to make sequencer 3 the lowest priority. Because we are using just one sequencer, we just need to make sure each sequencer has a unique priority. We set bits 15–12 (EM3) in the ADC_EMUX_R register to specify how the ADC will be triggered. If we specify software start (EM3=0x0), then the software writes an 8 (SS3) to the ADC_PSSI_R to initiate a conversion on sequencer 3. Bit 3 (INR3) in the ADC_RIS_R register will be set when the conversion is complete. We can enable and disable the sequencers using the ADC_ACTSS_R register. There are 11 on the TM4C123/LM4F120. Which channel we sample is configured by writing to the ADC_SSMUX3_R register. The ADC_SSSCTL3_R register specifies the mode of the ADC sample. Clear TS0. We set IE0 so that the INR3 bit is set on ADC conversion, and clear it when no flags are needed. We will set IE0 for both interrupt and busy-wait synchronization.

When using sequencer 3, there is only one sample, so END0 will always be set, signifying this sample is the end of the
sequence. Clear the D0 bit. The ADC_RIS_R register has flags that are set when the conversion is complete, assuming the IE0 bit is set. Do not set bits in the ADC_IM_R register because we do not want interrupts. Write one to ADC_ISC_R to clear the corresponding bit in the ADC_RIS_R register.

UART0 pins are on PA1 (transmit) and PA0 (receive). The UART0_IBRD_R and UART0_FBRD_R registers specify the baud rate. The baud rate divider is a 22-bit binary fixed-point value with a resolution of $2^{-6}$. The Baud16 clock is created from the system bus clock, with a frequency of $(\text{Bus clock frequency})/\text{divider}$. The baud rate is

$$\text{Baud rate} = \frac{\text{Baud16}}{16} = \frac{(\text{Bus clock frequency})}{16 \times \text{divider}}$$

We set bit 4 of the UART0_LCRH_R to enable the hardware FIFOs. We set both bits 5 and 6 of the UART0_LCRH_R to establish an 8-bit data frame. The RTRIS is set on a receiver timeout, which is when the receiver FIFO is not empty and no incoming frames have occurred in a 32-bit time period. The arm bits are in the UART0_IM_R register. To acknowledge an interrupt (make the trigger flag become zero), software writes a 1 to the corresponding bit in the UART0_IC_R register.

We set bit 0 of the UART0_CTL_R to enable the UART. Writing to UART0_DR_R register will output on the UART. This data is placed in a 16-deep transmit hardware FIFO. Data are transmitted first come first serve. Received data are place in a 16-deep receive hardware FIFO. Reading from UART0_DR_R register will get one data from the receive hardware FIFO.

The status of the two FIFOs can be seen in the UART0_FR_R register (FF is FIFO full, FE is FIFO empty). The standard name for the UART0 ISR is UART0_Handler. RXIFLSEL specifies the receive FIFO level that causes an interrupt (010 means interrupt on $\geq \frac{1}{2}$ full, or 7 to 8 characters). TXIFLSEL specifies the transmit FIFO level that causes an interrupt (010 means interrupt on $\leq \frac{1}{2}$ full, or 9 to 8 characters).

<table>
<thead>
<tr>
<th>$4000.\text{C}00$</th>
<th>31–12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7–0</th>
<th>Name</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>OE</td>
<td>BE</td>
<td>PE</td>
<td>FE</td>
<td>DATA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$4000.\text{C}04$</td>
<td>31–3</td>
<td>3</td>
<td>2</td>
<td>1</td>
<td>0</td>
<td>UART0_RSR_R</td>
<td></td>
</tr>
<tr>
<td></td>
<td>OE</td>
<td>BE</td>
<td>PE</td>
<td>FE</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$4000.\text{C}18$</td>
<td>TXFE</td>
<td>RXFF</td>
<td>TXFF</td>
<td>RXFE</td>
<td>BUSY</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$4000.\text{C}24$</td>
<td>31–16</td>
<td>15–0</td>
<td></td>
<td></td>
<td>DIVINT</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$4000.\text{C}28$</td>
<td>31–6</td>
<td>5–0</td>
<td></td>
<td></td>
<td>DIVFRAC</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$4000.\text{C}2C$</td>
<td>31–8</td>
<td>7</td>
<td>6–5</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>SPS</td>
<td>WPEN</td>
<td>FEN</td>
<td>STP2</td>
<td>EPS</td>
<td>PEN</td>
<td>BRK</td>
</tr>
<tr>
<td>$4000.\text{C}30$</td>
<td>31–10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6–3</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td></td>
<td>RXE</td>
<td>TXE</td>
<td>LBE</td>
<td>SIROL</td>
<td>SIREN</td>
<td>UARTEN</td>
<td></td>
</tr>
<tr>
<td>$4000.\text{C}34$</td>
<td>31–6</td>
<td>5–3</td>
<td>2–0</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>RXIFLSEL</td>
<td>TXIFLSEL</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$4000.\text{C}38$</td>
<td>31–11</td>
<td>10</td>
<td>9</td>
<td>8</td>
<td>7</td>
<td>6</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>OEIM</td>
<td>BEIM</td>
<td>PEIM</td>
<td>FEIM</td>
<td>RTIM</td>
<td>TXIM</td>
<td>RXIM</td>
</tr>
<tr>
<td>$4000.\text{C}3C$</td>
<td>OERIS</td>
<td>BERIS</td>
<td>PERIS</td>
<td>FERIS</td>
<td>RTRIS</td>
<td>TXRIS</td>
<td>RXRIS</td>
</tr>
<tr>
<td>$4000.\text{C}40$</td>
<td>OEMIS</td>
<td>BEMIS</td>
<td>PEMIS</td>
<td>FEMIS</td>
<td>RTMIS</td>
<td>TXMIS</td>
<td>RXMIS</td>
</tr>
<tr>
<td>$4000.\text{C}44$</td>
<td>OEIC</td>
<td>BEIC</td>
<td>PEIC</td>
<td>FEIC</td>
<td>RTIC</td>
<td>TXIC</td>
<td>RXIC</td>
</tr>
</tbody>
</table>

Table 11.2. UART0 registers. Each register is 32 bits wide. Shaded bits are zero.