Architectural Considerations for Network Processor Design

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Network Processor Background

- The Network Node Bottleneck
- Past: General Purpose Processors to ASICs
- Present: ASICs to Network Processors
  - Diverse Operations
  - Decreased Development Time and Cost
- Flexibility vs. Performance Trade Off
- Problem: Study Performance Enhancements and their Effects on the Flexibility of Network Processors

Previous Work: NP Design Issues

- Workload Characterization: Parallelism
- Parallel Processing [Crowley, et al., 2000]
  - Superscalar
  - SMT, CMP
- Cache Effectiveness [Liu, 2001; Wolf, et al., 2000]
- Instruction Set Design [Halfill, 1999]
- Various Hardware Structures [Prakash, et al. 2001]

Moving Forward: The Project

- Computational Model
  - Nodes as NP Processing Elements
  - Edges as Interconnection
  - Tokens as Packets
- Properties of the NP System
  - Parallelism: Superscalar, SMT, CMP
- Properties of the Workload
  - Packet Dependencies - Interconnections
  - Packet Processing Time - Nodes
  - Packet Memory References - Resources