Predictive Block Dataflow Model for Parallel Computation

Vishal Mishra
Kursad Oney

Dataflow Architecture

- No PC, Locally controlled events
- Event: firing of "actor" by incoming data
- Main idea: whole program is dataflow graph, exploit inherent parallelism in programs
- Early Machines: TTDA, Monsoon, Manchester
- Advantages:
  - Hides memory latency
  - Synchronization overhead less
- Issues:
  - Slow clock
  - Poor temporal and spatial locality

Model of Computation

- 2-D array of processors with local memory on a single chip
- Tokens passed: [dest., instruction ptr, data]
- Blocks of instructions, coarse grained
- Data driven, owner computes rule
- Async operation or loosely sync
- Predictive: pre-fetching blocks of instructions
- Locality: block level
- Global address space: processor id & memory

Model of Computation

- Predictive prefetch: Co-processor, prefetches and broadcasts the block of instructions. De-coupled architecture
- Block level locality
- Proposed:
  - Devise algorithms for quicksort, graph coloring