Node Prefetch Prediction in Dataflow Graphs

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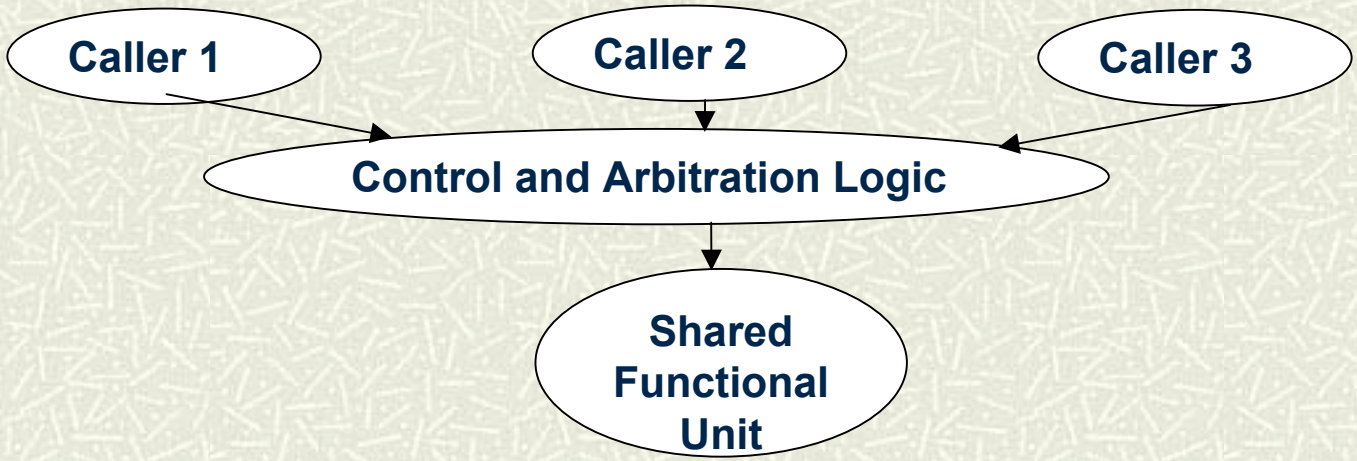
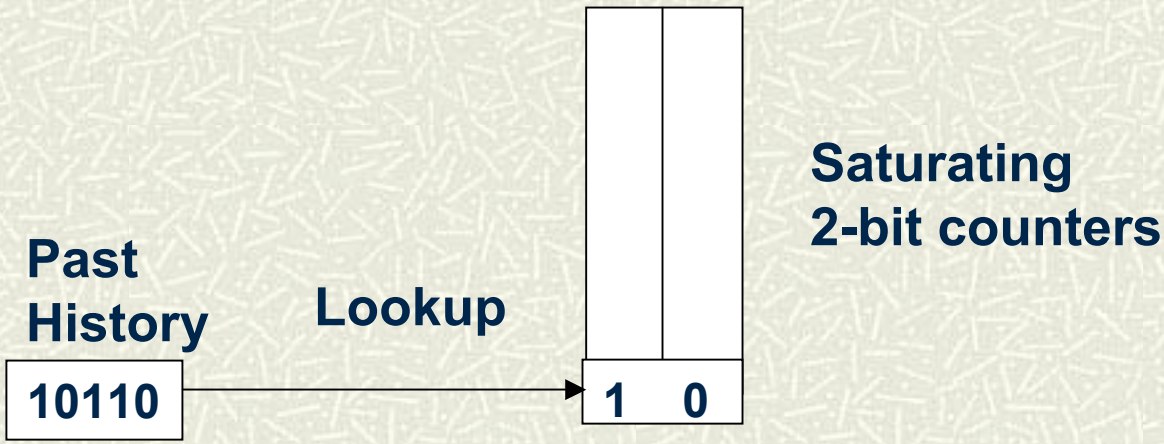
Caller Prediction

- Mutli-channel, dynamic measurement applications
  - Shared functional units
- Dynamically predict caller and prefetch state data
  - Parallel execution on dedicated hardware (FPGA)



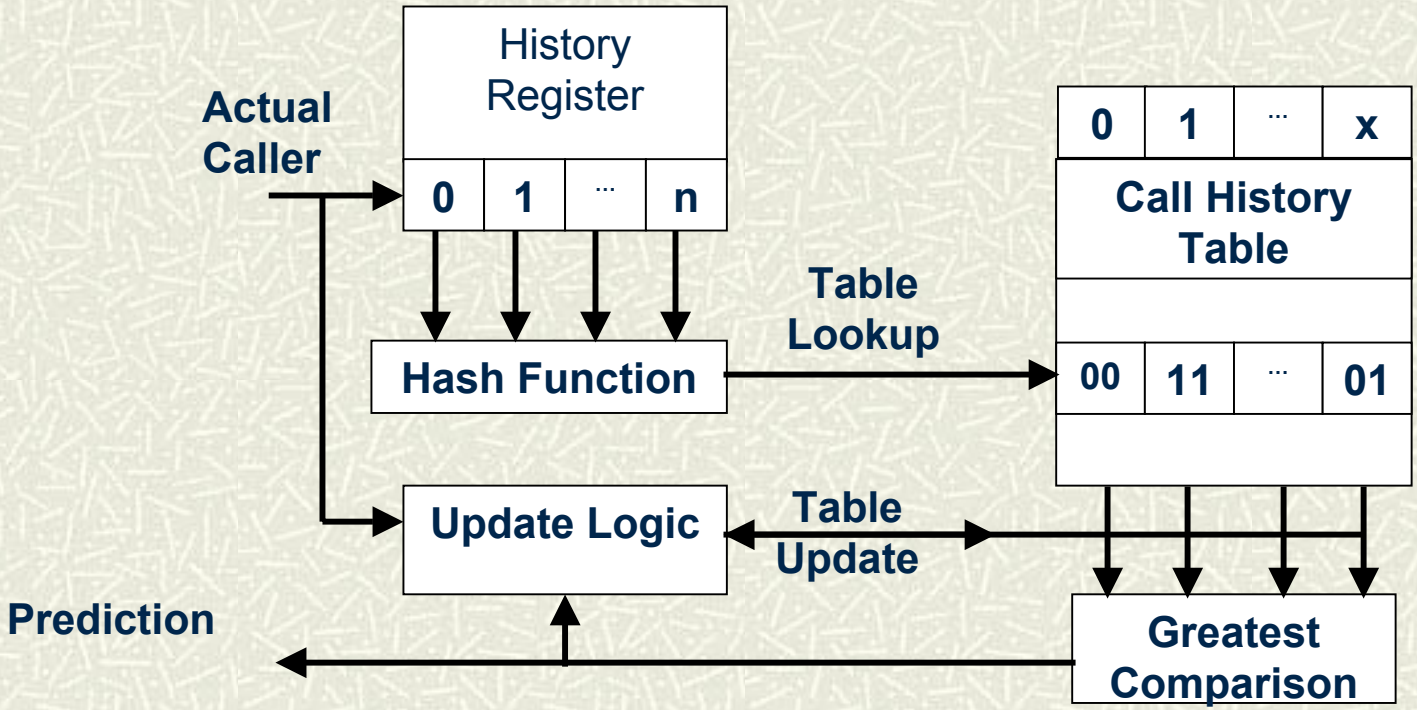
Approach

- Build on two level branch prediction
- History register
  - Indicates a taken branch
- Counter predicts a taken branch



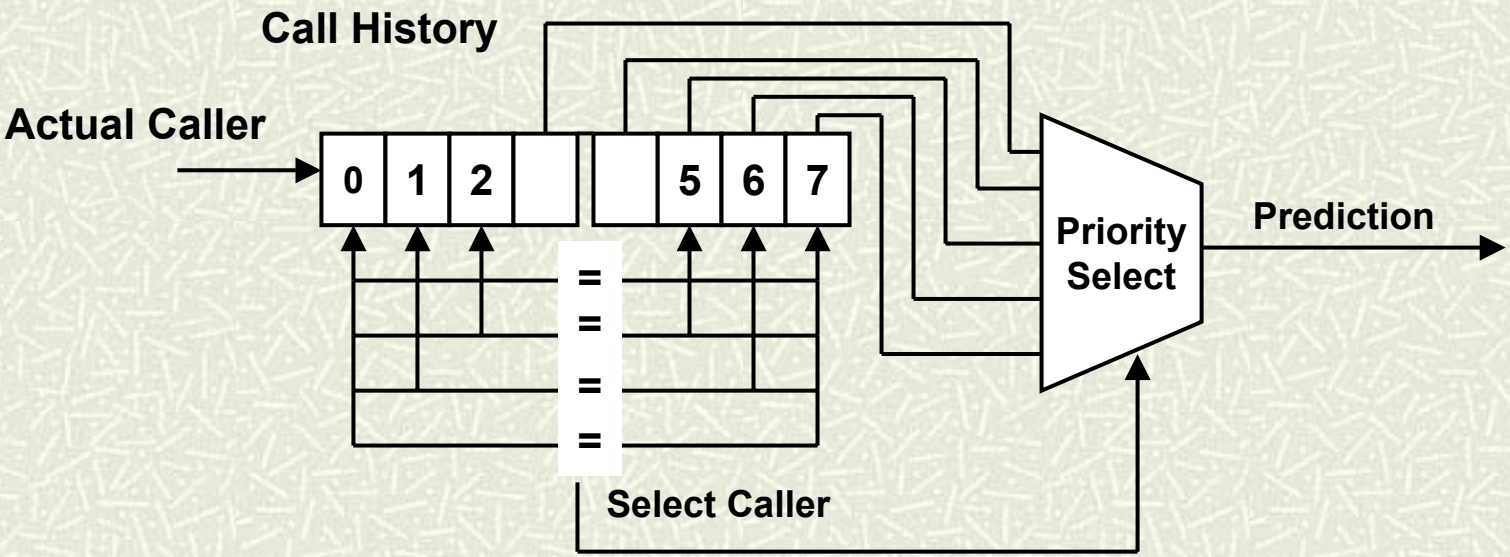
Solution – Two Level Predictor

- Call history table length - x^n
- Hash function



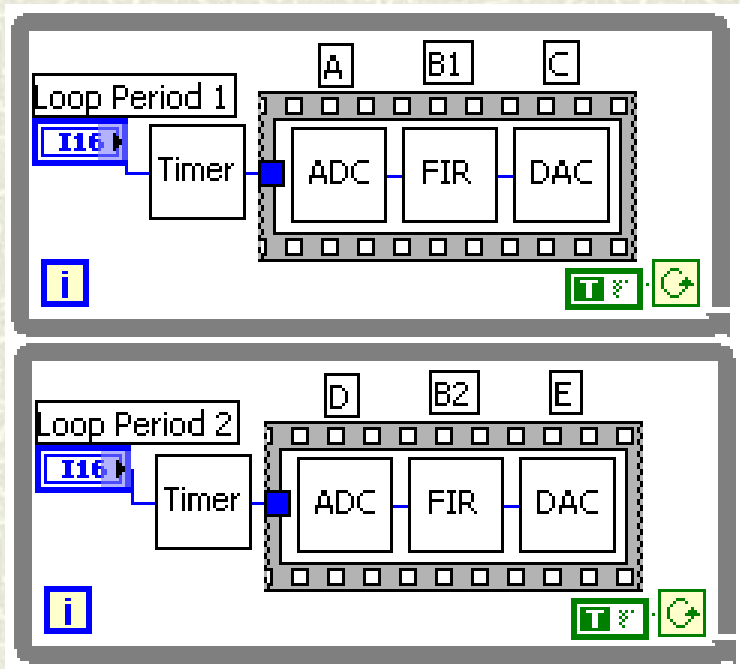
Period Detection Model

- Finds periodic behavior in current calling history
- Cheap to implement



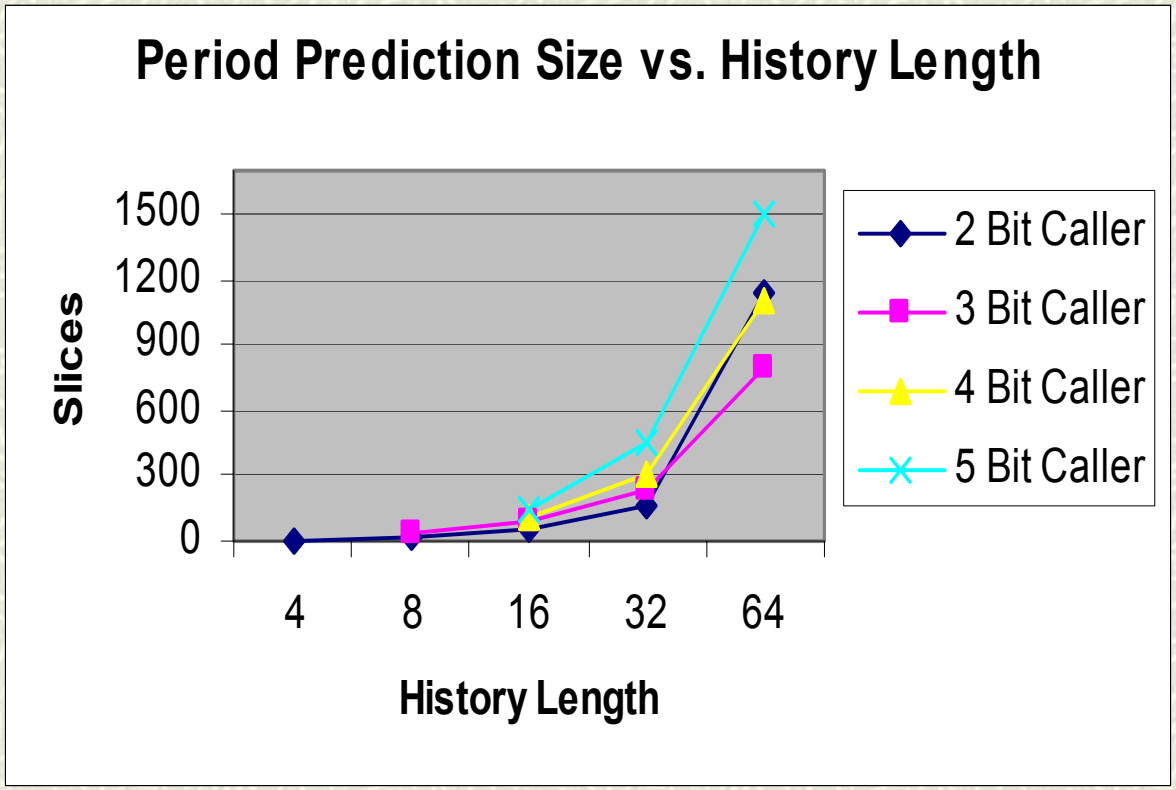
Evaluation - Sample Application

- LabVIEW application
- Shared FIR block
- Dynamic ADC sampling rate
- 33% faster with prediction



Hardware Cost

- Two level predictor
  > 500 slices
- 32 tap FIR
  360 slices



Conclusion

- Xilinx Virtex II™ FPGA implementation
- Shared nodes common in multi-channel measurement and control systems
- Two mechanisms for implementing caller prediction