

Designing Intelligent Surveillance Camera System

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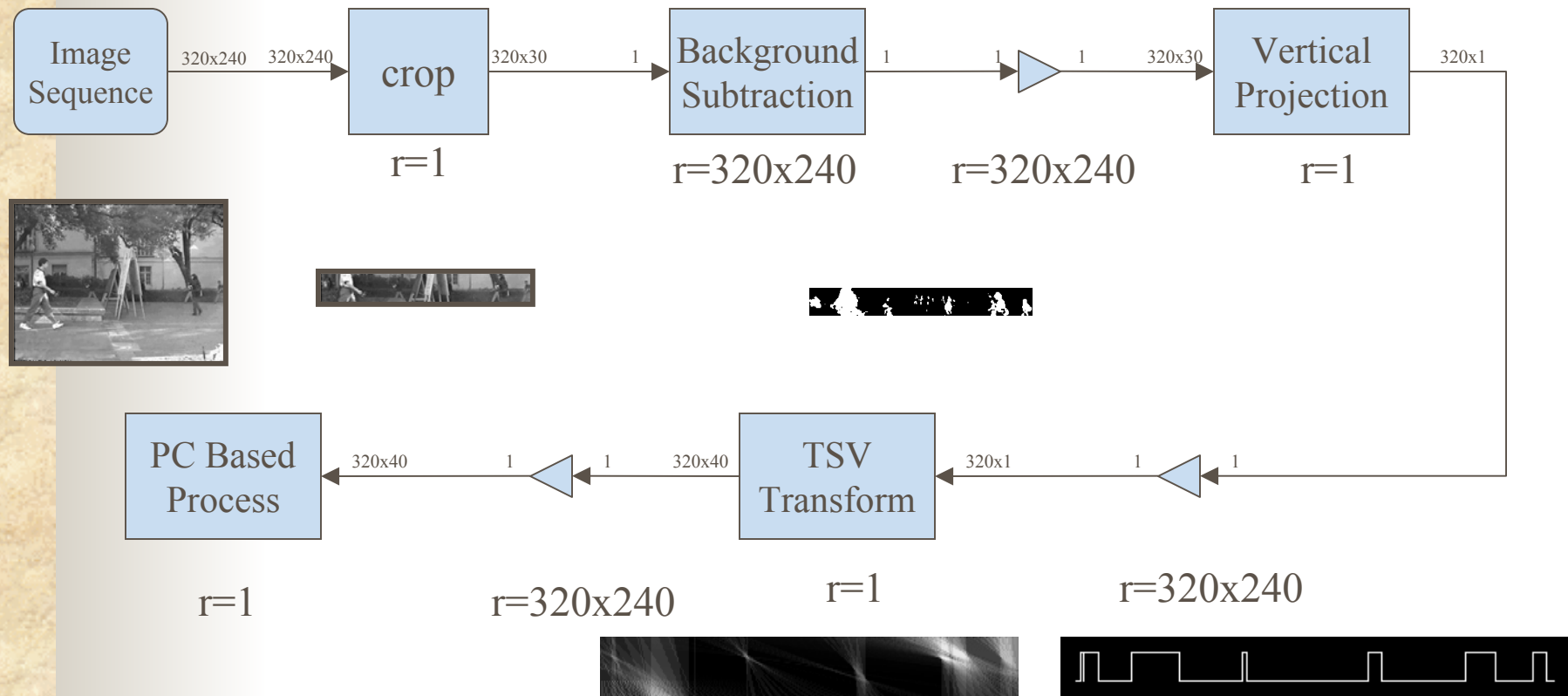
EE382C: Embedded Software Systems
Class Project: Final Presentation



Problem Statement

- Design an intelligent surveillance system
 - Preprocess for human tracking and human interaction recognition
 - Velocity extraction
 - Human segmentation
- Camera Features
 - Lateral view static monochrome camera
- Hybrid system
 - PC yields final results for whole system

Structure

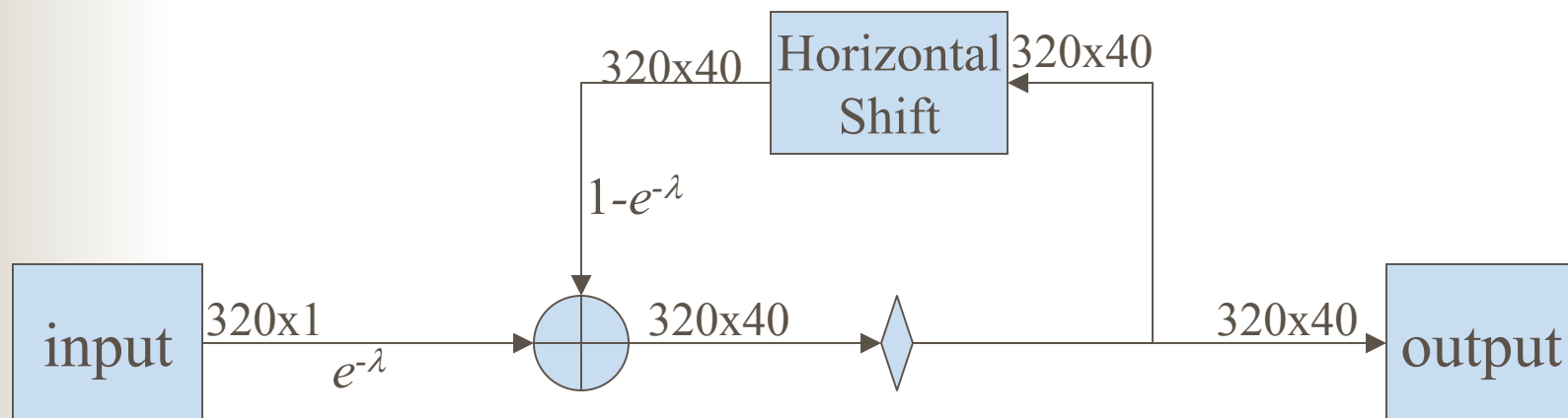


►Binarization process

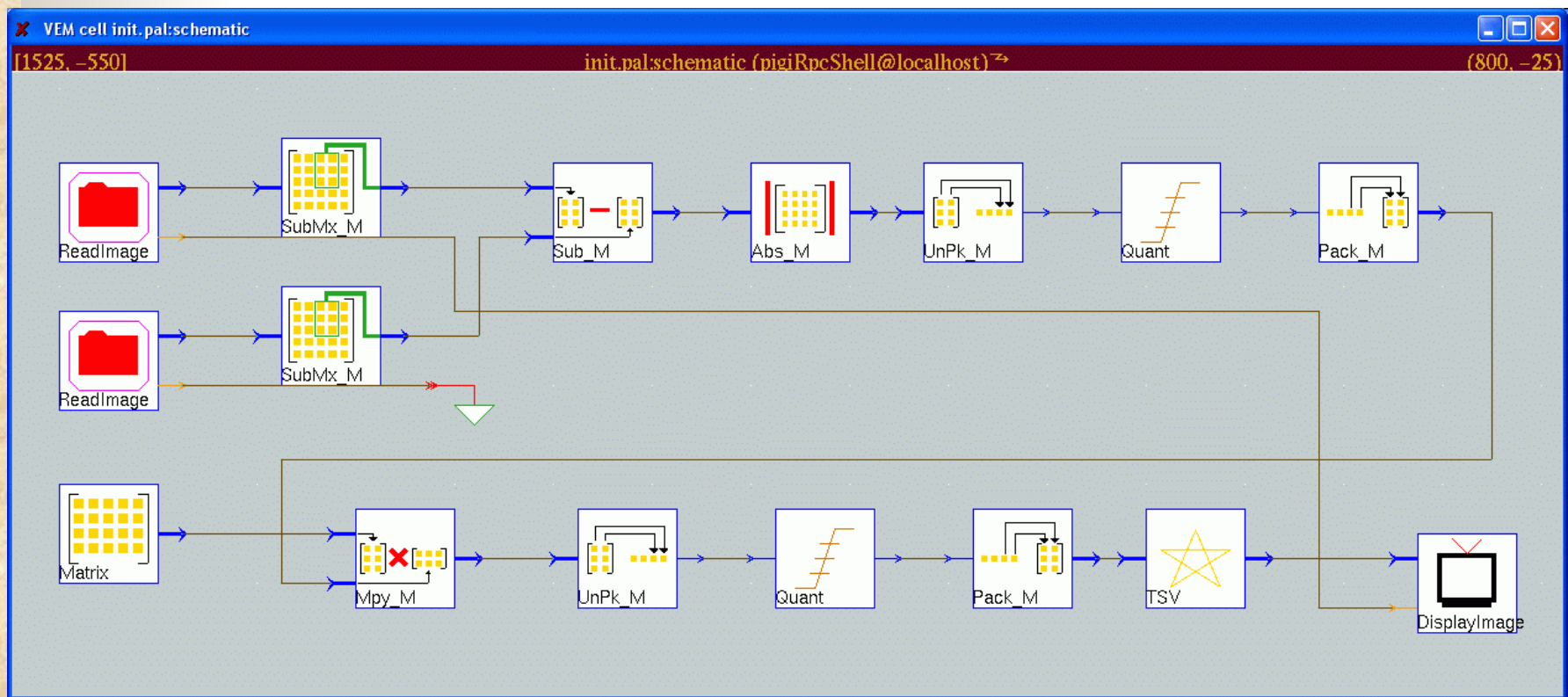
r : execution cycle per one frame cycle

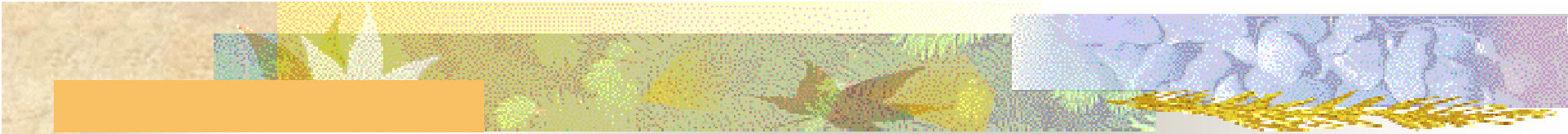
TSV Transform

- Extracts velocity from a sequence of one-dimensional binary images
 - Parallelogram shift (horizontal shift)
 - Multiplication / Addition



Design on Ptolemy





Simulation on Ptolemy

- Domain:
 - SDF
- Implementation
 - Stars in C++ / galaxy in dataflow programming
- Inputs
 - Sequence of PGM files (320x240 pixels)
 - 100 images in the sequence
- Output
 - Velocity extracted sequence of image (TSV image) :
PGM format (320x40 pixels)
 - 100 images in the sequence

Results



20th frame



40th frame



60th frame

Original
Image

TSV
Image

0

velocity

80th frame



100th frame



0

velocity

Original
Image

TSV
Image

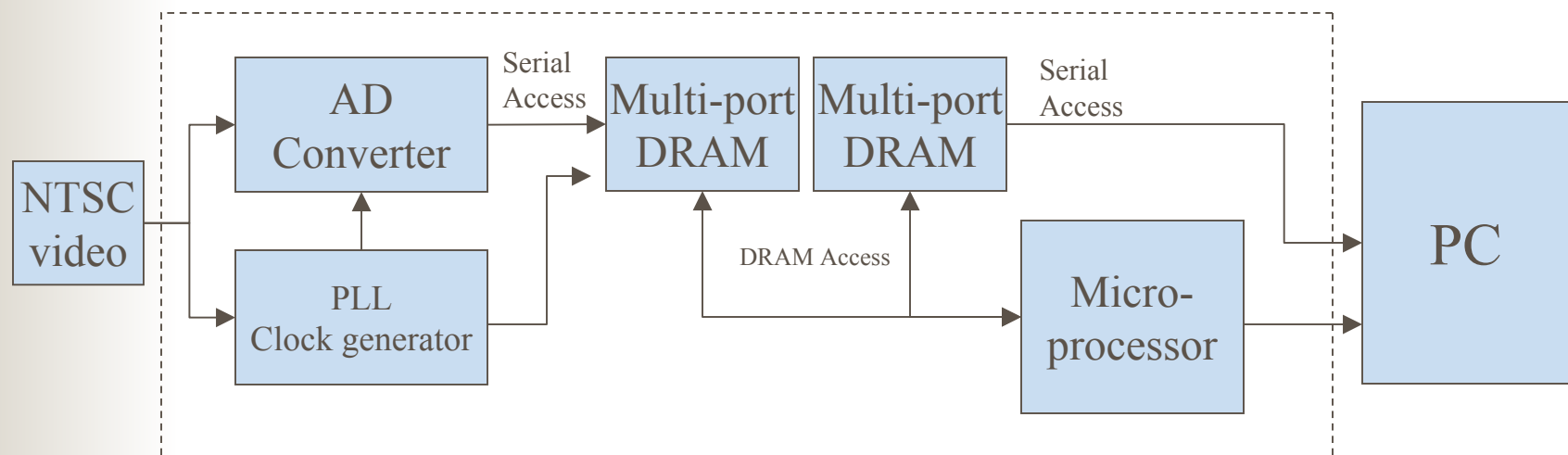
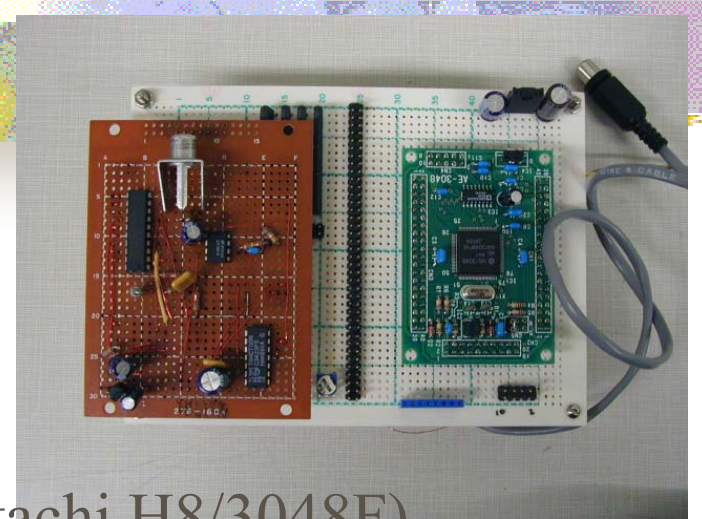
Simulation on microprocessor

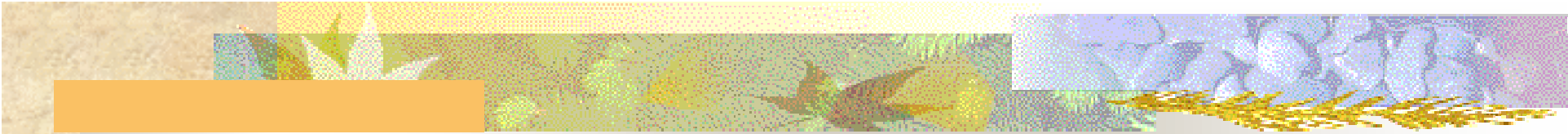
- Hardware Implementation

- 16bit CISC Microprocessor (Hitachi H8/3048F)
- Multi-port DRAM specialized for Image processing / Graphics (Mitsubishi M5M442256) (1Mbit x 4)

- Software Implementation

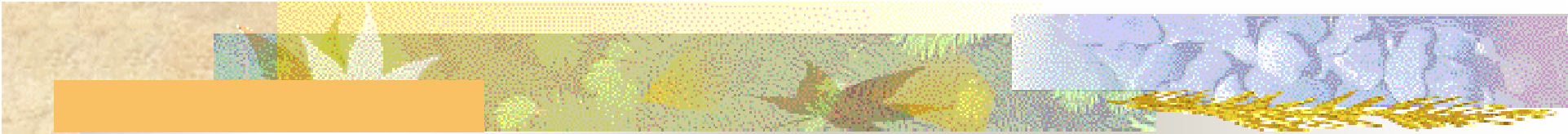
- C / Assembler





Result

- Computation time
89msec / cycle
 $< 100\text{msec} = 3 \text{ frame cycles}$
- Data rate to PC : 128kbps
- Code size : 5732 bytes
- Internal RAM usage (static) : 854 bytes



Conclusion

- Ptolemy Simulation
 - SDF: C / Data flow programming
- Hardware Simulation
 - 16 bit CISC Microprocessor / Multi-port DRAM
 - Fast computation (3 image frame cycles)with low power processor
 - Small code size
 - Small internal RAM size
- Future Work
 - DSP Simulation on Ptolemy
 - DSP Implementation on hardware