

# EE382m — Logic Synthesis

## Midterm

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Name:

Topic	Question	Max Marks	Your Marks
<i>Algebraic optimizations</i>	Q1.a	13	
	Q1.b	12	
<i>Don't Cares</i>	Q2	25	
<i>Technology Mapping</i>	Q3.a	5	
	Q3.b	20	
Total		75	

1. Algebraic multilevel minimization

(a) [13 marks]

Suppose we represented functions at internal nodes of a multilevel logic network by BDDs (as opposed to sums-of-products or factored forms).

Taking the cost of a node to be the number of nonconstant BDD nodes in its function, how would you perform elimination on such a network?

(b) [12 marks]

Compute all the kernels of the following algebraic expression:

$$d * z + c * z + b * z + a * z + d * y + c * y + b * y + a * y + d * x + c * x + b * x + a * x$$

Note—the expression is the product of  $(a + b + c + d)$  with  $(x + y + z)$ , and this fact should help you come up with the kernels without having to go through the tedious algorithm we discussed in class.

## 2. Node minimization

[25 marks]

(a) Compute the SDC for the 3-input AND gate whose variable is  $F$  in Figure 1, in terms of its immediate fanins. What is the simplest function you can replace the 3-input NOR gate by? (Do not actually change it.)

(b) Compute the ODC for the node  $u$  in terms of the primary input space, and simplify it as much as possible.

Now compute the ODC for the node  $v$  in terms of the primary input space, and simplify it as much as possible. (Keep in mind that the function at node  $u$  has changed because of the previous optimization.)

Now compute the ODC for the node  $w$  in terms of the primary input space, and simplify it as much as possible. (Keep in mind that the function at nodes  $u$  and  $v$  have changed because of the previous optimizations.)

(c) What is the simplest function from the inputs  $a, b, c$  to  $u, v, w$  that can be substituted for the existing logic, without changing overall input-output functionality? (I.e., what's the simplest circuit that can take the place of the logic in the hatched rectangle?)

(d) Why is the circuit you got from part (c) not the same as the circuit from part (d)?

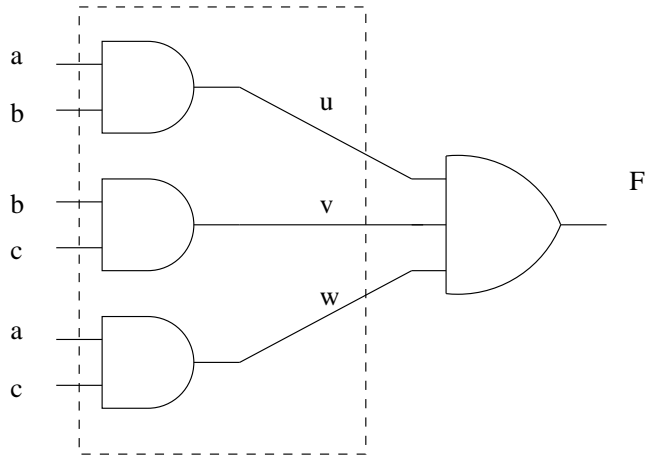


Figure 1: A multilevel logic circuit.

### 3. Technology mapping

(a) [5 marks]

We saw how to exactly solve the minimum area technology mapping problem for arbitrary designs using binate covering (where we had a Boolean variable  $m_i$  for each match, and set up constraints requiring that each gate in the subject graph be covered, etc.).

Why then did we study the tree-based approach, which required decomposing the subject graph into trees?

(b) [20 marks]

How would you modify the Dynamic Programming based procedure for minimum area mapping of trees to obtain a mapping procedure that computes for each possible arrival time for the output, the least area mapping that achieves that delay? The delay model is very simple—each gate in the library has a delay of 1. (Assume the primary inputs all arrive at time 0.)

How does the time complexity of your procedure compare to that of the minimum area mapping algorithm?