EE360R: Term Papers *[DRAFT]*

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Introduction

There are three reasons you should take the term paper seriously:

1. It is worth 10% of your grade (but this should be the least important item),
2. it will give you training on how to go about reading and learning from technical literature, and
3. you will gain insight into a specific real-world VLSI design effort.

The goal of this paper is to report on one of the papers from the list I've attached. You may choose a separate paper on your own, but be sure to run your selection by me for approval before you commit to it.

You should related the paper to the various aspects of the design to what you learned in class. You should also critique the design—point out what you feel are flaws in the design, e.g., poor choices of circuit style, not enough attention to verification, targeting a nonexistent market, etc. Basically, I want you to **think hard** about what your read.

Bear in mind that in order to do this in a meaningful way, you will have to read beyond just the paper you selected, e.g., the class text, citations within the paper you chose, IEEE Spectrum, etc.

In high school, assembling paragraphs from different papers into a term paper is the norm. However, I will view copying material verbatim to be plagiarism, unless it is clearly cited and presented for a good reason.

Timeline

Progress reports

I would like you to provide in class a one to two page summary on the status of your report on the following days:

1. November 3 (If you are choosing a paper outside of the list, you need to have approval for it by this date.)
2. November 15

Final report

The final report is due 5:00pm on the last day of classes (December 3)

Evaluation

Your grade on the project will be based on a number of factors, particularly the originality and quality of your ideas. Other considerations include writing and attention to detail.

Suggested Papers

You can access papers from the*IEEE Journal of Solid State Circuits* online at the following URL:

`http://ieeeexplore.ieee.org/xpl/RecentIssue.jsp?puNumber=4`

(You will need to be on a UT computer.)

- Processors

  - The implementation of the Itanium-2 microprocessor. *IEEE Journal of Solid State Circuits.* November 2002. Pages 1448–1460.
  - Implementation of a third-generation 1.1-GHz 64-bit microprocessor. *IEEE Journal of Solid State Circuits.* November 2002. Pages 1461–1469.
  - A 1.5-GHz 130-nm Itanium-2 Processor with 6-MB on-die L3 cache. *IEEE Journal of Solid State Circuits.* November 2003. Pages 1887–1895.
  - A 1.3-GHz fifth-generation SPARC64 microprocessor. *IEEE Journal of Solid State Circuits.* November 2003. Pages 1896–1905.

- Datapath

  - 5-GHz 32-bit integer execution core in 130-nm dual-Vt/CMOS. *IEEE Journal of Solid State Circuits.* November 2002. Pages 1421–1432.
  - A fully bypassed six-issue integer datapath and register file on the Itanium-2 microprocessor. *IEEE Journal of Solid State Circuits.* November 2002. Pages 1433–1440.
  - A shared-well dual-supply-voltage 64-bit ALU. *IEEE Journal of Solid State Circuits.* March 2004. Pages 494–500.

- Embedded systems

  - A reconfigurable system featuring dynamically extensible embedded microprocessor, FPGA, and customizable I/O. *IEEE Journal of Solid State Circuits.* March 2003. Pages 521-529.
  - A 2× load/store pipe for a low-power 1-GHz embedded processor. *IEEE Journal of Solid State Circuits.* November 2003. Pages 1857–1865.
  - A VLIW processor with reconfigurable instruction set for embedded applications. *IEEE Journal of Solid State Circuits.* November 2003. Pages 1876–1886.

- Networking

  - A TCP offload accelerator for 10 Gb/s Ethernet in 90-nm CMOS. *IEEE Journal of Solid State Circuits.* November 2003. Pages 1866–1875.
  - A 400-MT/s 6.4-GB/s multiprocessor bus interface. *IEEE Journal of Solid State Circuits.* November 2003. Pages 1846–1856.

- Communications/DSP

  - A 64-point Fourier transform chip for high-speed wireless LAN application using OFDM. *IEEE Journal of Solid State Circuits.* March 2004. Pages 484–493.
  - Design Considerations and Implementation of a DSP-Based Car-Radio IF Processor. *IEEE Journal of Solid State Circuits.* July 2004. Pages 1110–1118.
  - A single-chip MPEG-2 codec based on customizable media embedded processor. *IEEE Journal of Solid State Circuits.* March 2003. Pages 530–540.