EE 360R — Computer-aided IC Design, Unique No. 15885 Fall 2004
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Office Hours: MW 1:00-2:00pm Lecture: MW 3:30-5:00, ENS 127

Description:

We aim to study the process of implementing a digital system as a CMOS integrated circuit.

The course will begin with a review of the basics of CMOS transistor operation and the manufacturing process for CMOS VLSI chips.

We will then study in detail the problem of implementing logic gates in CMOS. Specifically, we will cover layout, design rules, and circuit families.

Afterwards, we will examine techniques for timing and power analysis and clocking. We will also examine ways to optimize timing and power. This will be followed by an overview of datapath design, specifically adders and multipliers. We will also study memory arrays, including SRAM and DRAM cell and clock design.

The course will conclude with a survey level treatment of advanced topics, including functional verification, test, design-for-test, electrical effects, and future trends.

We will also have guest lecturers talk about real-world design practise.

Prerequisites:

This course is intended for ECE undergraduate students. A knowledge of digital logic design (EE316 or its equivalent), and Computer Architecture (EE360N, or its equivalent) is required.

Recommended text:

- CMOS VLSI Design: A Circuits and Systems Perspective. N. Weste and D. Harris. *3rd Edition*, 2004. Addison-Wesley.

Web site:

All material related to the course is available at `www.ece.utexas.edu/~adnan`

Format/Evaluation:

I will assign approximately 6 written homeworks, which will consist of questions from the book, and will be worth 10% of your grade. There will be three in-class tests collectively worth 50% of your grade. There will be three major design projects which will count for 30% of your grade. The remaining 10% of your grade will be based on a term paper, due on the last day of classes, in which you will be asked to critique a commercial design effort.

Tentative Outline

Week	Material
	Preliminaries
Aug 25	Introduction, history
Aug 30	MOS transistor theory
Sep 1	CMOS processing
Sep 6	Labor day—no class
Sep 8	Layout 1
	CMOS circuit and logic design
Sep 13	Basic logic design in CMOS, Lab 1 posted
Sep 15	Basic physical design
Sep 20	Dynamic CMOS
Sep 22	Adders
Sep 27	Midterm 1
	Timing
Sep 29	Circuit characterization
Oct 4	Circuit characterization
Oct 6	Delay calculation, Lab 1 due, Lab 2 posted
Oct 11	Performance optimization
Oct 13	Performance optimization
	Control
Oct 18	Control design
Oct 20	Midterm 2
Oct 25	Latches and clocking, Lab 2a due
Oct 27	Verilog and synthesis
	Datapath and memories
Nov 1	MOS memories, Lab 2b due, Lab 3 posted
Nov 3	MOS memories
Nov 8	Floating point
	Advanced topics
Nov 10	Test
Nov 15	Verification
Nov 22	Midterm 3
Nov 24	Wed before Thanksgiving = no class ?
Nov 29	Electrical considerations
Dec 1	Conclusion, Lab 3 due, term paper due

NOTE: All departmental, college and university regulations concerning drops will be followed. The University of Texas at Austin provides upon request appropriate academic adjustments for qualified students with disabilities. For more information, contact the Office of the Dean of Students at 471-6259, 471-4241 TDD.