EE360R — Midterm 1.b

Spring 2003

Name:

- Max marks = 50, Time = 50 mins
- Open book, open notes
- Write your answers on the exam
- Show your work and give explanations

1. Explain the term “self aligned gate process.”

3 marks

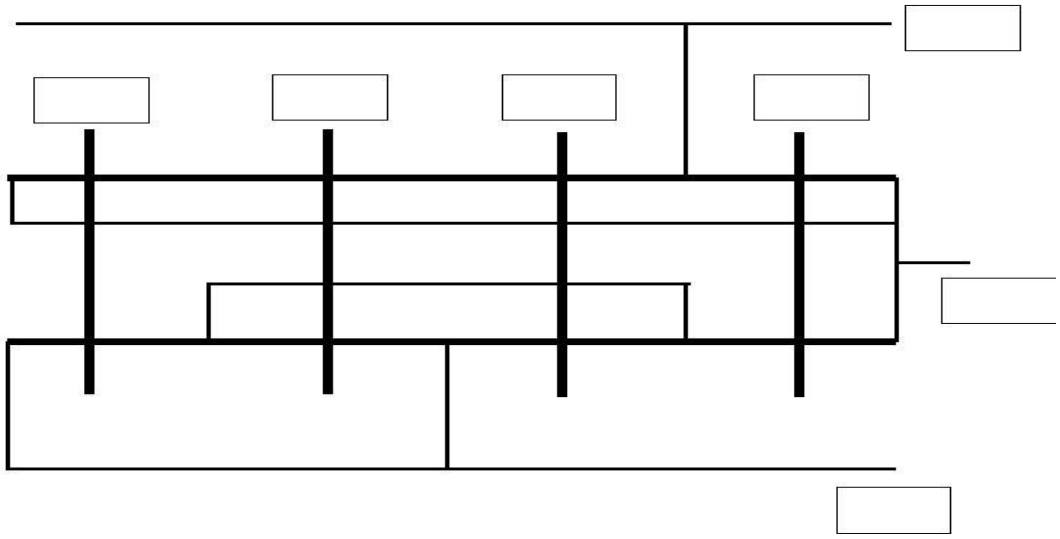
2. Consider an NMOS transistor in a 1.2μm CMOS process. The transistor width is 2.4μm, and length is 1.2μm. The threshold voltage is 0.75V.

   Suppose the manufacturing process could result in a 15% variation in the threshold voltage, a 10% variation in the oxide thickness, and a 0.12μm variation in the width and in the length, for the actual device that is fabricated.

   Assume that $V_{GS} = V_{DS} = 4V$. What is the ratio of the maximum value of the drain current to the minimum value of the drain current for the fabricated device?

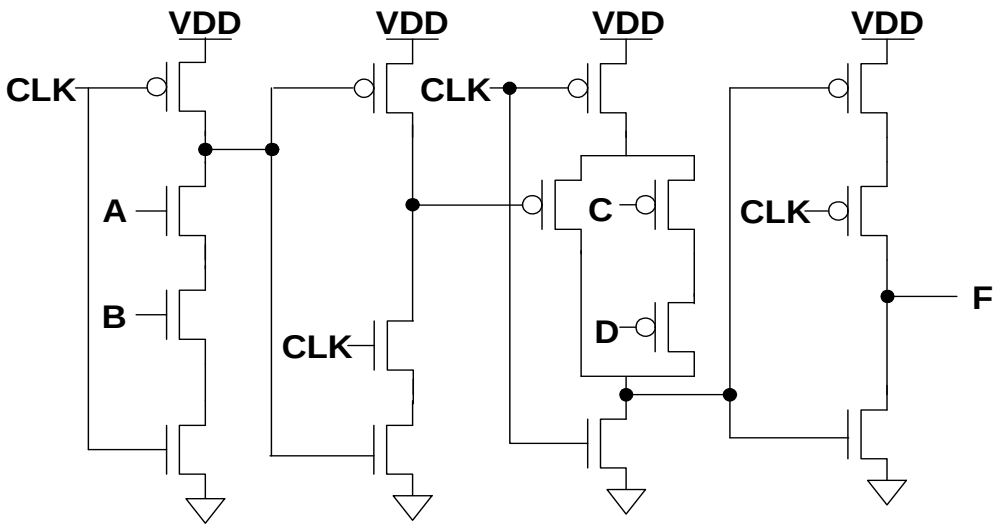
10 marks

3. Label the inputs to the following circuit so that the circuit implements the following logic function $F = \overline{(P + Q + R) \cdot S}$. Explain why your labeling is correct.



12 marks

4. Explain the operation of this circuit in terms of the clock phase, and write down the equation for its function.



11 marks

5. Implement the function $\overline{(X \cdot Y + Z \cdot Y + Z \cdot X)}$ as a single gate in the complementary static CMOS style in such a way both the pull-up and the pull-down networks have no more than 2 transistors connected in series.

14 marks