EE 360R — Computer-aided IC Design | Fall 2005
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Office Hours: MW 2:00-3:00pm | Lecture: MW 3:30-4:45pm, ENS 127

Description:

We aim to study the process of implementing a digital system as a CMOS integrated circuit.

The course will begin with a review of the basics of CMOS transistor operation and the manufacturing process for CMOS VLSI chips.

We will then study in detail the problem of implementing logic gates in CMOS. Specifically, we will cover layout, design rules, and circuit families.

Afterwards, we will examine techniques for timing and power analysis and clocking. We will also examine ways to optimize timing and power. This will be followed by an overview of datapath design, specifically adders and multipliers. We will also study memory arrays, including SRAM and DRAM cell and clock design.

The course will conclude with a survey level treatment of various peripheral topics, including functional verification, test, design-for-test, electrical effects, and future trends.

We will also have guest lecturers talk about real-world design practice.

Prerequisites:

This course is intended for ECE undergraduate students. A knowledge of digital logic design (EE316 or its equivalent), and Computer Architecture (EE360N, or its equivalent) is required.

Recommended text:

- Principles of CMOS VLSI Design. N. Weste and D. Harris. *3rd Edition*, 2005. Addison-Wesley.

Web site: All material related to the course is available at `www.ece.utexas.edu/~adnan`

Format/Evaluation:

I will assign approximately 6 written homeworks, which will consist of questions from the book, and will be worth 10% of your grade. There will be two in-class midterms and a final exam, collectively worth 60% of your grade. Three major design projects will make up the remainder of your grade.

Tentative Outline

Week	Material
	Preliminaries
Aug 31	Introduction, history
Sep 5	MOS transistor theory
Sep 7	MOS transistor theory
Sep 12	CMOS processing
Sep 14	Circuit characterization
	CMOS circuit and logic design
Sep 19	Basic logic gate design
Sep 21	Lab 1 & Basic physical design
Sep 26	Basic physical design
Sep 28	Circuit families-1
Oct 3	Circuit families-2
Oct 5	Latch design
Oct 10	Clocking-1
Oct 12	Midterm 1
Oct 17	Lab 2 & Clocking-2
	Datapath and memories
Oct 19	Datapath—adders
Oct 24	Datapath—multipliers
Oct 26	MOS memory arrays—1
Oct 31	MOS memory arrays—2
	Timing optimization
Nov 2	Timing analysis
Nov 7	Timing optimization
Nov 9	Lab 3 & RTL Synthesis
Nov 14	Midterm 2
	Topics
Nov 16	Verification
Nov 21	Testing
Nov 23	DFT
Nov 28	Clock trees, PLLs
Nov 30	I/O
Dec 5	Scaling-1
Dec 7	Scaling-2

NOTE: All departmental, college and university regulations concerning drops will be followed. The University of Texas at Austin provides upon request appropriate academic adjustments for qualified students with disabilities. For more information, contact the Office of the Dean of Students at 471-6259, 471-4241 TDD.