360R - Final

Name:

- Time = 180 mins, Max marks 111
- Closed book/notes; one crib sheet
- Write your answers on the exam
- Show your work and give explanations

Figures are shown on separate pages at the end.

Layout

The cross-sectional view of an inverter is given in Figure Cross-Section. Identify the various regions as being SiO2, Poly, Metal, VDD, Gnd, n+, p+, n-well, and p-substrate.

Transistor theory

Suppose you were to design an NMOS transistor in a 0.5μ m CMOS process. The transistor width is 2.0μ m, and length is 0.5μ m.

The manufacturing process could result in a 25% variation in the threshold voltage, a 20% variation in the oxide thickness, and a 0.1μ m variation in the width and in the length, for the actual device that is fabricated.

Assume that $V_{GS} = V_{DS} = 3V$; the threshold voltage is 0.5V.

What is the ratio of the maximum value of the drain current to the minimum value of the drain current that could flow through the fabricated device when it is in saturation?

Circuit families

1. What problem with dynamic logic does domino dynamic logic overcome, and what is the primary limitation of domino dynamic logic?

5 marks

2. Give a transistor level schematic for a domino logic implementation of the function $A \cdot B \cdot C \cdot D \cdot E \cdot F$. No domino gate should have more than two inputs.

(You are not required to specify devices sizes, just draw the transistors and the connections between them.)

Datapath

The FF1 ("find-first-one") function takes an *n*-bit input vector A[n-1:0], and returns and *n*-bit output B[n-1:0], where B[i] = 1 if and only if A[i] = 1 and for all j > i, A[j] = 0.

Describe how you would implement the "find-first-one" (FF1) function on n inputs using static gates, specifically 2-input NAND, 2 i/p NOR, and INVERTERS.

Credit will be given to *efficient* solutions.

Adders

Recall that a full-adder implements the following two logic equations:

$$C_{out} = A \cdot B + B \cdot C_{in} + A \cdot C_{in}$$
$$S_{out} = A \oplus B \oplus C_{in}$$

It is easy to show (e.g., by examining the truth table for these equations) that if the inputs to the full-adder are inverted, then so are the output. How can this fact be used to reduce the delay of a ripple-carry adder? Illustrate your reasoning on a 4-bit ripple carry adder.

Delay Analysis

Consider the circuit shown in Figure Delay-Analysis. From the plot of V_{out} vs. time, estimate the effective resistance of the NMOS transistor. (Assume that all the capacitance seen on the output of the inverter is lumped into C.)

\mathbf{RAMs}

1. Describe three **similarities** between SRAMs and DRAMs. What is the single biggest **difference** between an SRAM and DRAM? How do SRAMs and DRAMs **compare** in performance and in density?

2. Describe how you would use a 32 entry 8-bit word SRAM to implement a queue. Assume the queue read and writes are exclusive. Your queue has to signal whether it's full or empty. (You can use additional registers and logic.)

Test/Verification

1. How do scan flops help simplify the problem of manufacturing test?

4 marks

2. Suppose you were designing a microprocessor.

One approach to functionally verifying the processor is to ignore the internal units (e.g., the cache, the ALU, the pipeline control logic, et.c), and simply write large sets of test programs, and run them on both the RTL and the golder reference model (typically written in C).

What are the two most significant benefits to verifying the internal units additionally?

Deep Submicron

Suppose you were designing a chip in 45 nm technology, and you wanted to minimize power consumption.

The manufacturing process offers you two kinds of transistors—type F, which has a low V_T and a thin gate oxide, and type S, which has a high V_T and a thick gate oxide.

How do the type F and S transistors differ in terms of their power consumption and performance? How would you exploit them to reduce power in your design? (Be specific.)