VLSI-1 — Midterm 2

Fall 2005

Name:

- Max marks = 74, Time = 75 mins
- Open book/notes
- Write your answers on the exam
- Show your work and give explanations

Figures are shown on a separate page at the end.

Interconnect

The aspect ratio of a wire is the ratio of its thickness to its width.

Twenty years ago, wire aspect ratios used to be much less than 1; now they are greater than 1. What caused this change?

5 marks

Circuits

Each of circuits in Figure 1 (a)–(f) is observed to fail to operate as expected.

For each part of this question, the symptom is given.

- You are to explain the *cause* of the failure, and propose a *solution*.

1. The 2-1 mux in Figure 1 (a) works correctly when $V_{DD} = 2$ Volts. However, when $V_{DD} = 1.2$ Volts, when the selected input is logic 0 it works correctly, but not when the selected input is logic 1.

2. For the dynamic AND gate in Figure 1 (b), in the evaluate phase the output always eventually becomes 1.

3. For the OR gate in Figure 1 (c), if two or more inputs are logic 1, the output is logic 1; if all the inputs are logic 0, the output is logic 0; and if exactly one of the inputs is logic 1, the output is logic 0.

4. For the latch in Figure 1 (d), when the input D comes from a gate far away on the chip, the output remains stuck-at-1, regardless of D and EN.

5. For the AND gate in Figure 1 (e), in the evaluate phase with inputs A and B set to logic 0, the output goes to logic 1.

6. For the latch in Figure 1 (f), the output is seen to change even if the enable signal is low when the data input comes from a far-away gate.

24 marks

Adders

Consider the design of a 16-bit adder, with a carry-in.

Assume you have the individual G_i and P_i signals, and the only gate in your library is a 4 input 2 output gate that computes $(g_a + p_a \cdot g_b, p_a \cdot p_b)$.

1. Derive a circuit that computes the group generate ($G_{15:0}$) and propagate ($P_{15:0}$) signals—use as few levels of logic as possible.

12 marks

2. In order to implement the adder, you need all the group generate and propagate signals, i.e., $G_{i:0}$ and $P_{i:0}$ for $i = 0$ to 15. What trade-offs do you have to make between area (measured by number of gates) and delay (measured by number of levels of logic)?

13 marks

Sequential design

1. Many industrial designs use 2-phase latches, with the two latch clocks ϕ_1 and ϕ_2 driven by clk and $c\bar{l}k$ respectively.
   - Explain how this takes away one of the advantages of 2-phase clocking.

   7 marks

   - Suggest why this is done—specifically, what advantage does such a scheme have over combining latches into flops, and using just clk.

   8 marks

2. Latches used in pulsed-mode clocking have been described as "fast flops with lousy hold times." Explain what this means.

   5 marks